Intel® Pentium® III and FC-PGA Celeron™ Processor/815E Chipset
Universal Socket 370 Platform
Customer Reference Board Schematics

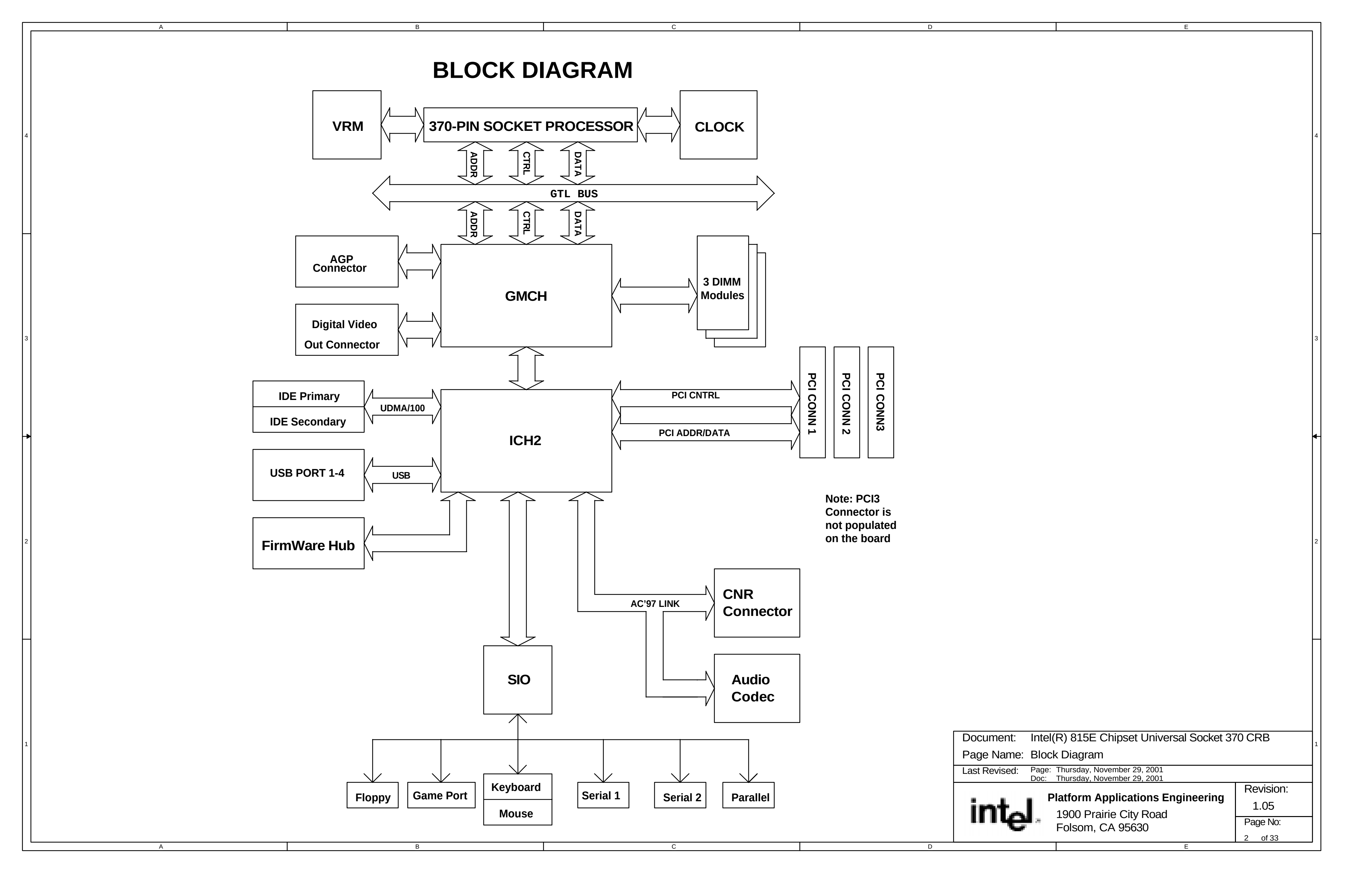
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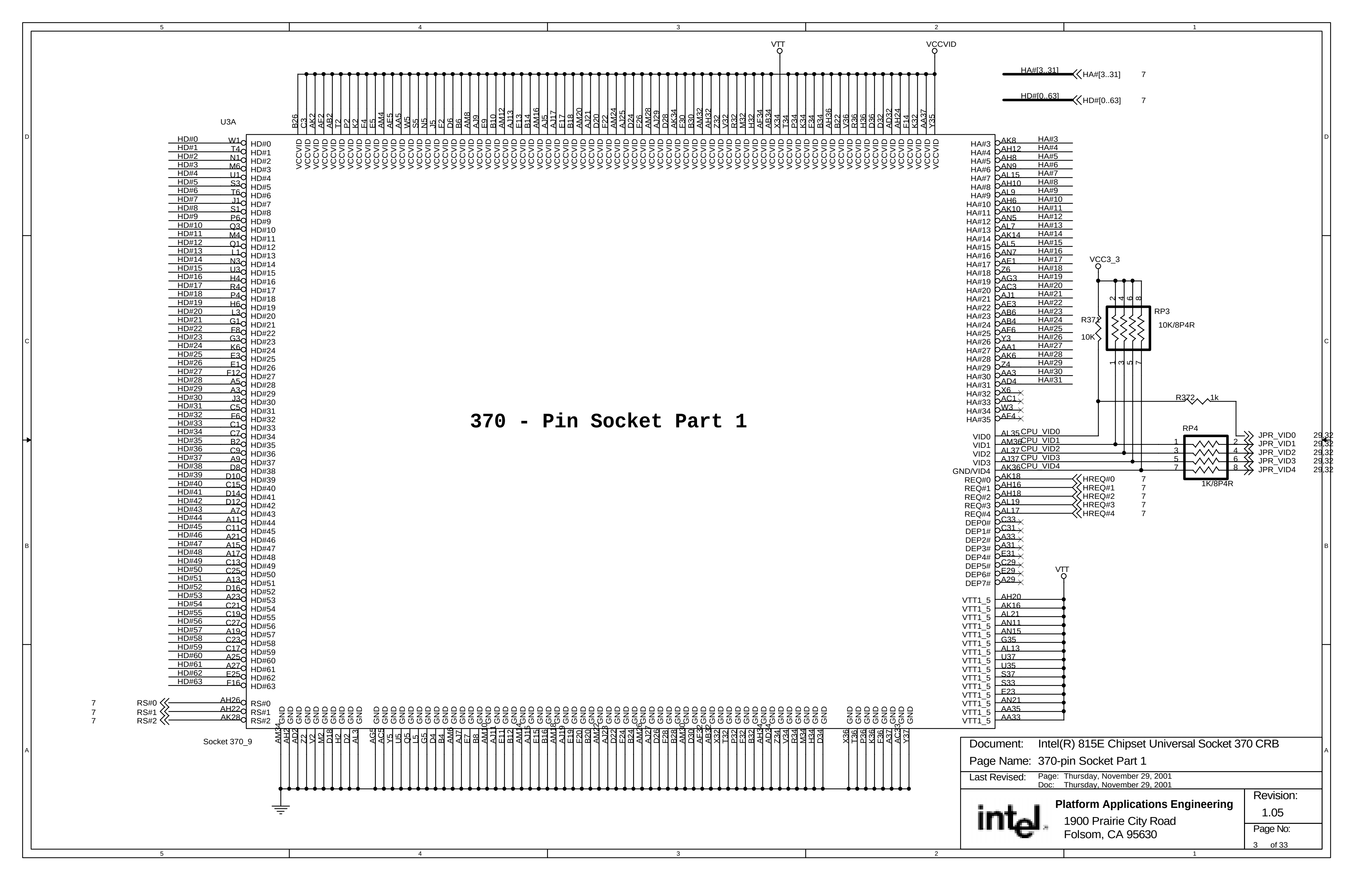
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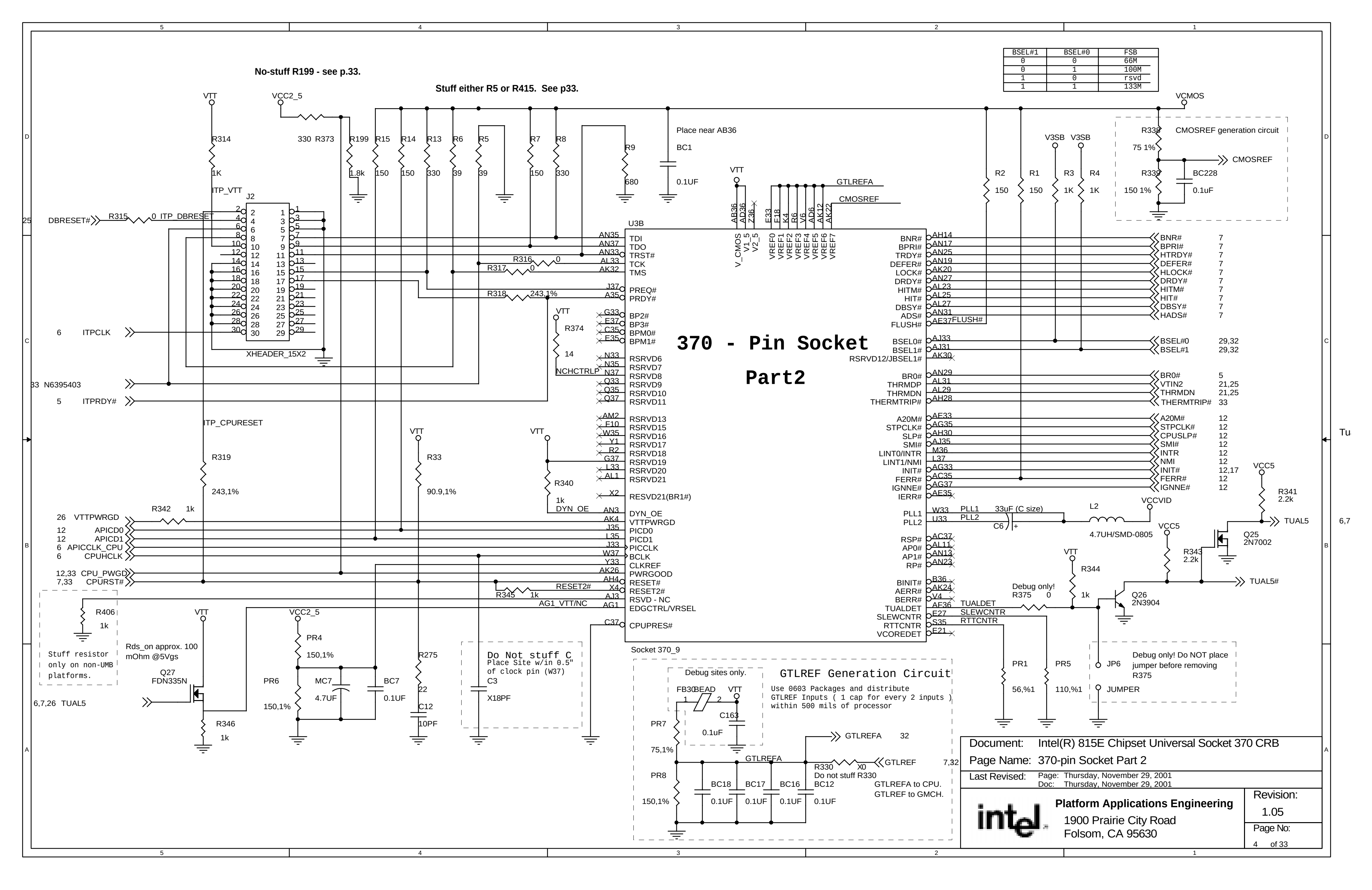
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Page Name:	Block Diagram
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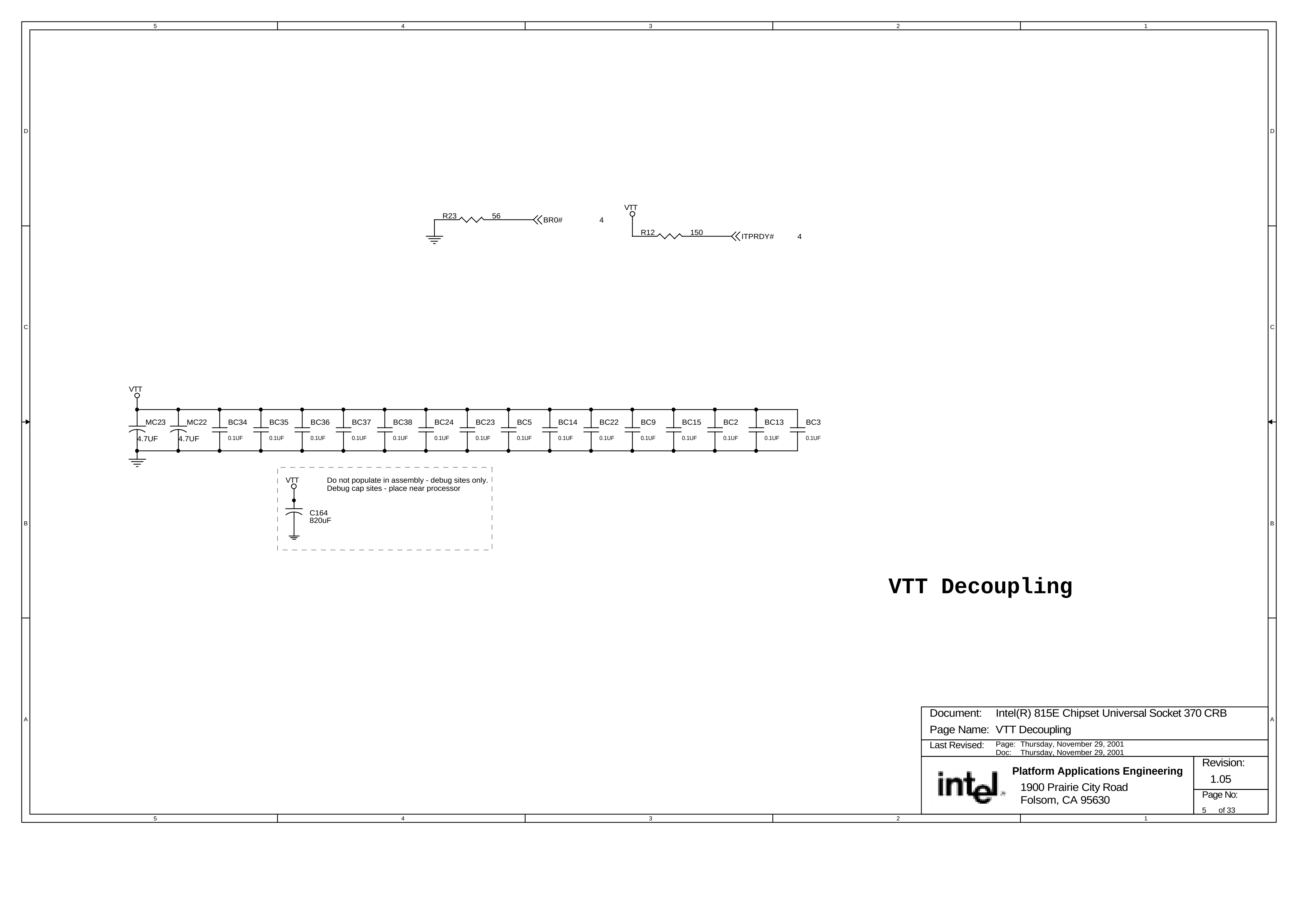

370 - Pin Socket Part 1
U3A
Socket 370_9
VTT
VCCVID
HA#[3..31]
HD#[0..63]
VCC3_3
R371
10K
RP3
10K/8P4R
R372
1k
RP4
1K/8P4R
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
JPR_VID0
JPR_VID1
JPR_VID2
JPR_VID3
JPR_VID4
VID0
VID1
VID2
VID3
GND/VID4
HREQ#0
HREQ#1
HREQ#2
HREQ#3
HREQ#4
REQ#0
REQ#1
REQ#2
REQ#3
REQ#4
DEP0#
DEP1#
DEP2#
DEP3#
DEP4#
DEP5#
DEP6#
DEP7#
VTT1_5
RS#0
RS#1
RS#2
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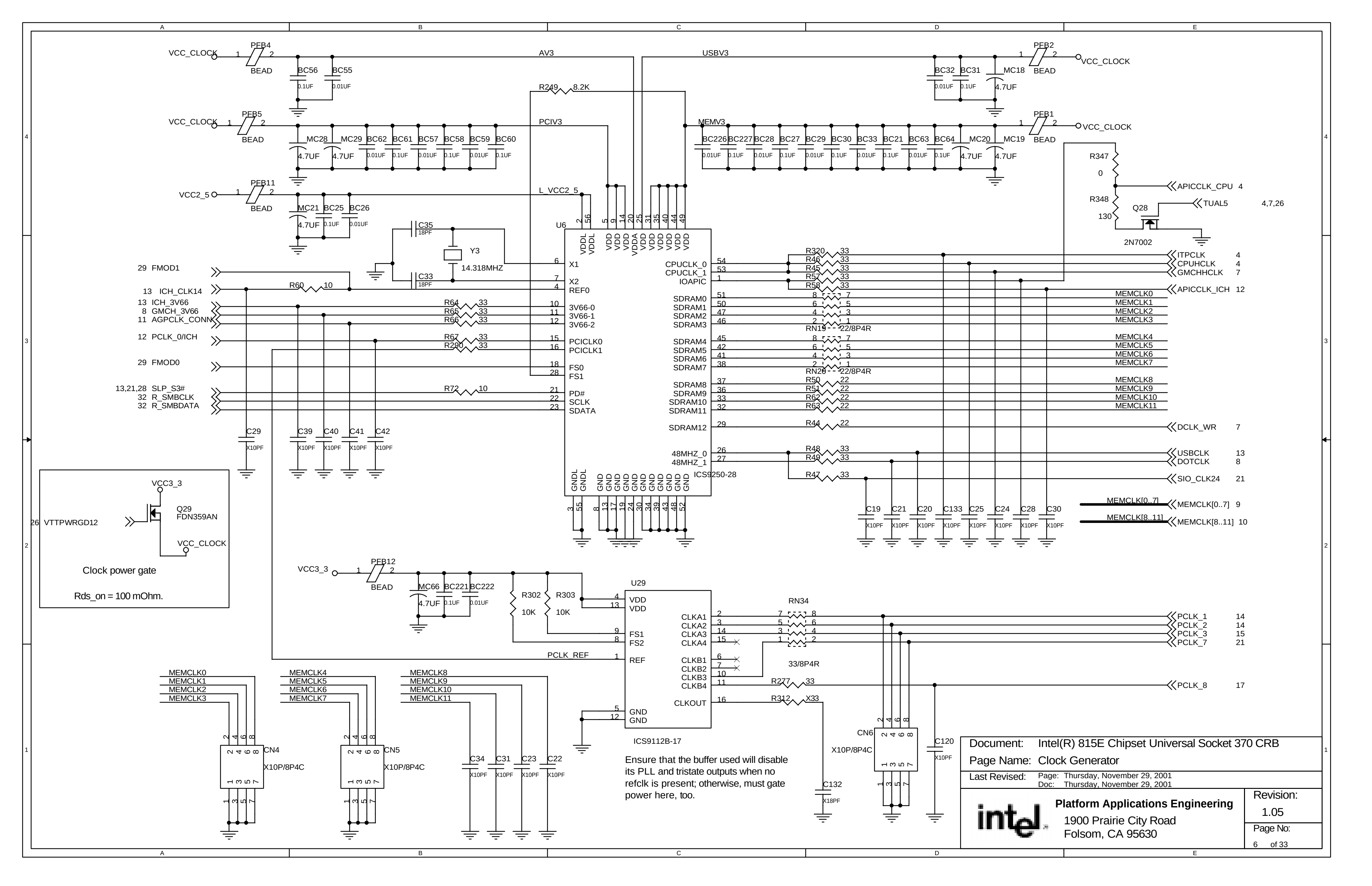
BSEL#1	BSEL#0	FSB
0	0	66M
0	1	100M
1	0	rsvd
1	1	133M

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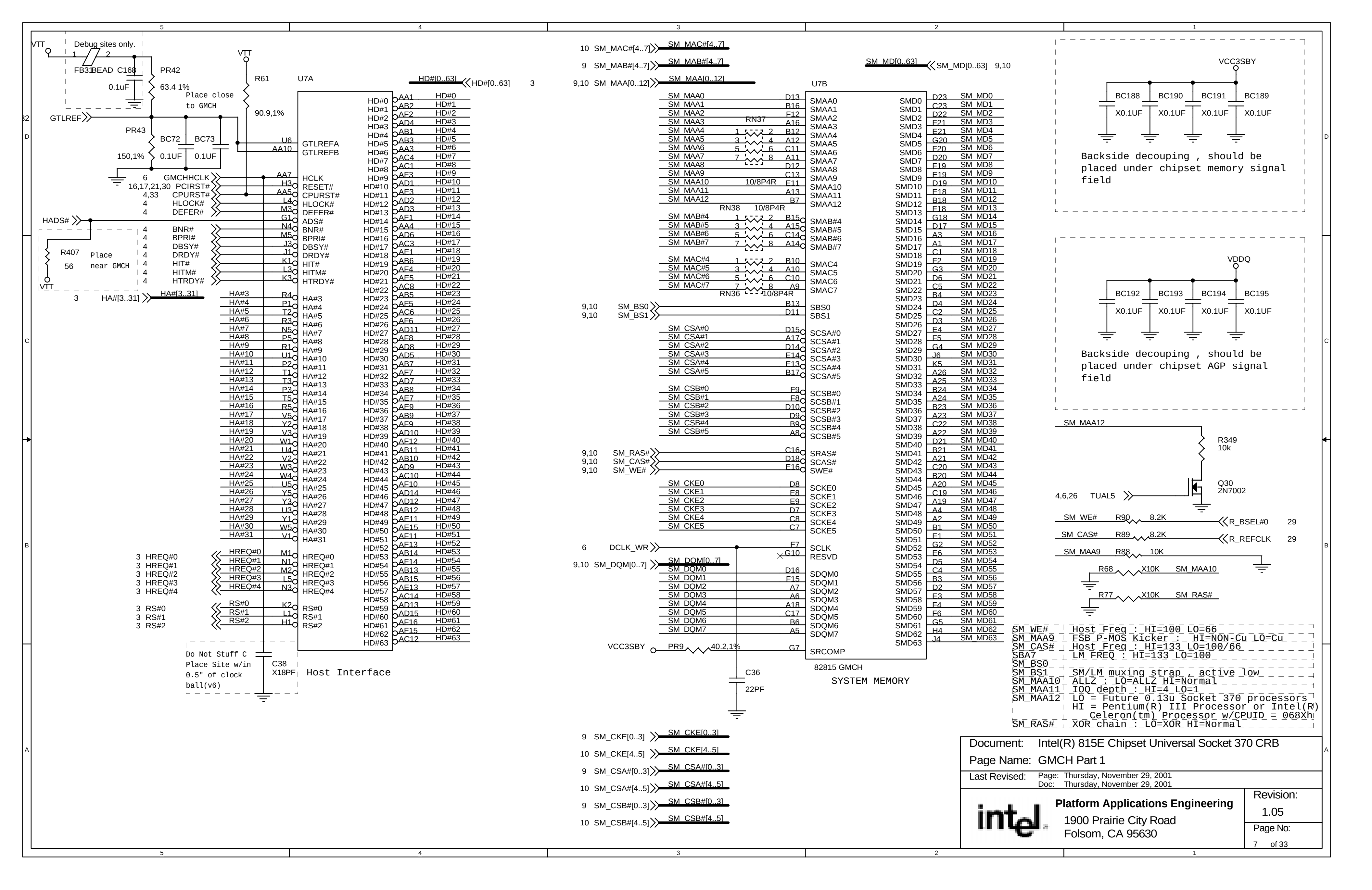
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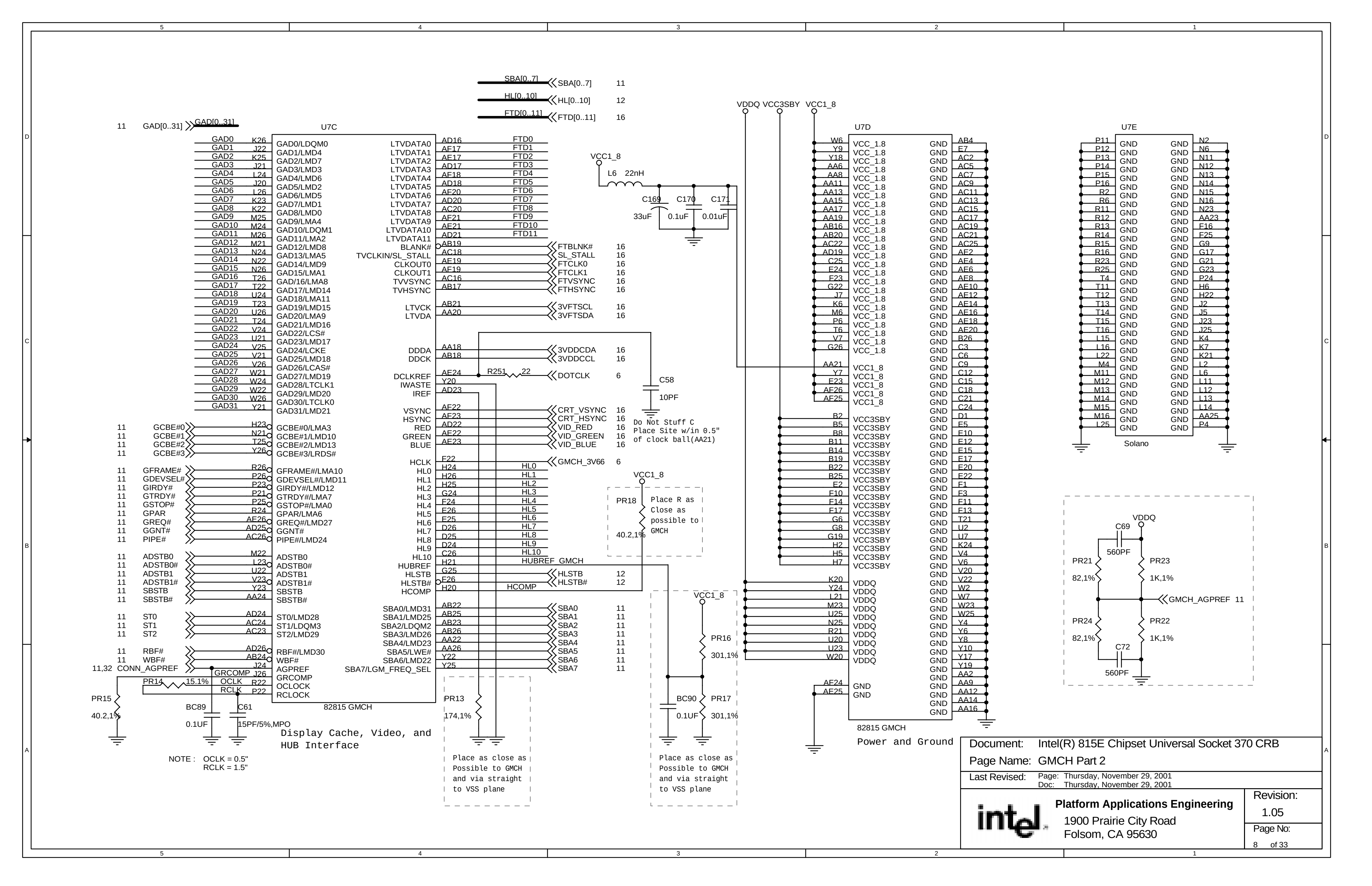
R23 56 BR0# 4
VTT
R12 150 ITPRDY# 4
VTT
MC23 4.7UF
MC22 4.7UF
BC34 0.1UF
BC35 0.1UF
BC36 0.1UF
BC37 0.1UF
BC38 0.1UF
BC24 0.1UF
BC23 0.1UF
BC5 0.1UF
BC14 0.1UF
BC22 0.1UF
BC9 0.1UF
BC15 0.1UF
BC2 0.1UF
BC13 0.1UF
BC3 0.1UF
VTT
Do not populate in assembly - debug sites only.
Debug cap sites - place near processor
C164 820uF
VTT Decoupling
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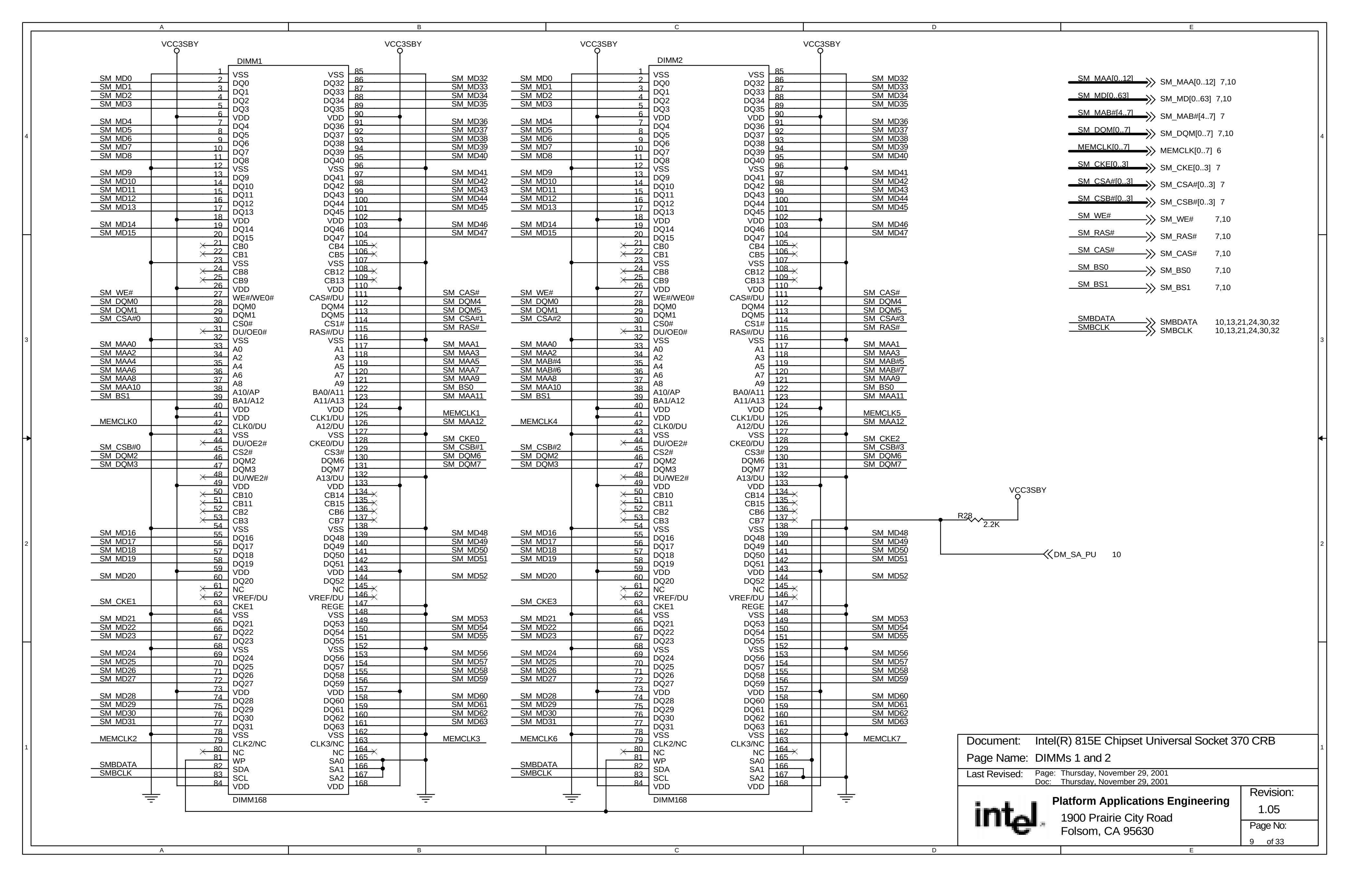


VCC_CLOCK
FB4
BEAD
BC56
BC55
AV3
USBV3
FB2
VCC_CLOCK
BC32
BC31
MC18
4.7UF
R249
8.2K
VCC_CLOCK
FB5
PCIV3
MEMV3
FB1
MC28
MC29
BC62
BC61
BC57
BC58
BC59
BC60
BC226
BC227
BC28
BC27
BC29
BC30
BC33
BC21
BC63
BC64
MC20
MC19
R347
0
VCC2_5
FB11
L_VCC2_5
MC21
BC25
BC26
APICCLK_CPU 4
R348
130
Q28
TUAL5
4,7,26
2N7002
C35
18PF
Y3
14.318MHZ
C33
U6
X1
X2
REF0
3V66-0
3V66-1
3V66-2
PCICLK0
PCICLK1
FS0
FS1
PD#
SCLK
SDATA
VDDL
VDD
VDDA
CPUCLK_0
CPUCLK_1
IOAPIC
SDRAM0
SDRAM1
SDRAM2
SDRAM3
SDRAM4
SDRAM5
SDRAM6
SDRAM7
SDRAM8
SDRAM9
SDRAM10
SDRAM11
SDRAM12
48MHZ_0
48MHZ_1
GNDL
GND
ICS9250-28
29 FMOD1
13 ICH_CLK14
R60 10
13 ICH_3V66
8 GMCH_3V66
11 AGPCLK_CONN
R64 33
R65 33
R66 33
12 PCLK_0/ICH
R67 33
R290 33
29 FMOD0
13,21,28 SLP_S3#
32 R_SMBCLK
32 R_SMBDATA
R72 10
C29
C39
C40
C41
C42
X10PF
R320 33
R46 33
R45 33
R57 33
R58 33
ITPCLK 4
CPUHCLK 4
GMCHHCLK 7
APICCLK_ICH 12
RN19 22/8P4R
RN20 22/8P4R
MEMCLK0
MEMCLK1
MEMCLK2
MEMCLK3
MEMCLK4
MEMCLK5
MEMCLK6
MEMCLK7
R50 22
R51 22
R62 22
R63 22
MEMCLK8
MEMCLK9
MEMCLK10
MEMCLK11
R44 22
DCLK_WR 7
R48 33
R49 33
USBCLK 13
DOTCLK 8
R47 33
SIO_CLK24 21
C19
C21
C20
C133
C25
C24
C28
C30
MEMCLK[0..7]
MEMCLK[0..7] 9
MEMCLK[8..11]
MEMCLK[8..11] 10
VCC3_3
Q29
FDN359AN
26 VTTPWRGD12
VCC_CLOCK
Clock power gate
Rds_on = 100 mOhm.
VCC3_3
FB12
BEAD
MC66
4.7UF
BC221
BC222
R302
10K
R303
10K
U29
VDD
FS1
FS2
REF
PCLK_REF
GND
CLKA1
CLKA2
CLKA3
CLKA4
CLKB1
CLKB2
CLKB3
CLKB4
CLKOUT
ICS9112B-17
RN34
33/8P4R
PCLK_1 14
PCLK_2 14
PCLK_3 15
PCLK_7 21
R277 33
PCLK_8 17
R312 X33
C132
X18PF
CN6
X10P/8P4C
C120
CN4
X10P/8P4C
CN5
X10P/8P4C
C34
C31
C23
C22
Ensure that the buffer used will disable its PLL and tristate outputs when no refclk is present; otherwise, must gate power here, too.
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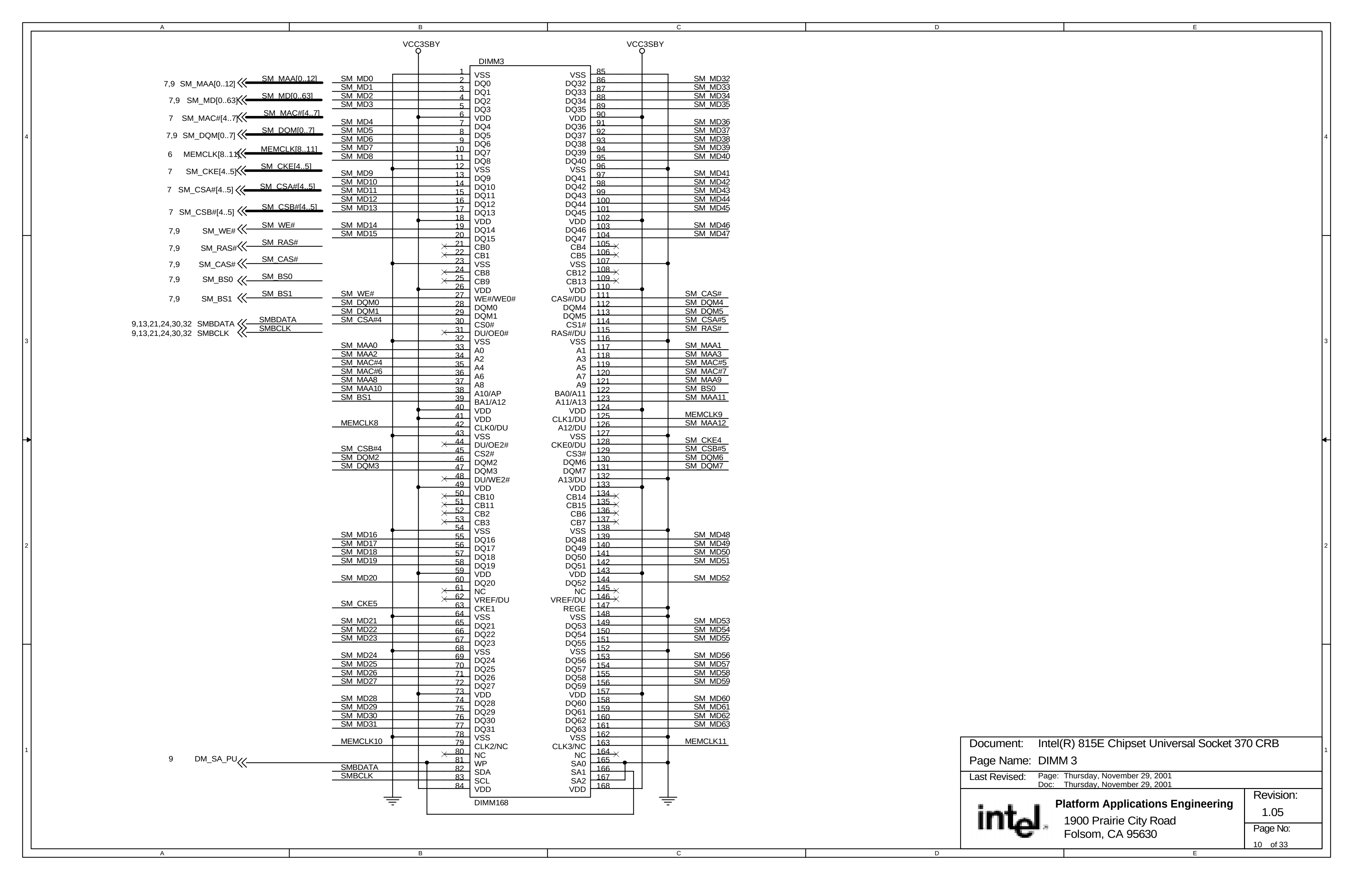
Debug sites only.
VTT
FB31 BEAD C168 0.1uF
PR42 63.4 1%
Place close to GMCH
R61 90.9,1%
GTLREF
PR43 150,1%
BC72 0.1UF
BC73 0.1UF
U7A
HD#[0..63]
6 GMCHHCLK
16,17,21,30 PCIRST#
4,33 CPURST#
4 HLOCK#
4 DEFER#
HADS#
4 BNR#
4 BPRI#
4 DBSY#
4 DRDY#
4 HIT#
4 HITM#
4 HTRDY#
R407 56 Place near GMCH
3 HA#[3..31]
GTLREFA
GTLREFB
HCLK
RESET#
CPURST#
HLOCK#
DEFER#
ADS#
BNR#
BPRI#
DBSY#
DRDY#
HIT#
HITM#
HTRDY#
3 HREQ#0
3 HREQ#1
3 HREQ#2
3 HREQ#3
3 HREQ#4
3 RS#0
3 RS#1
3 RS#2
Do Not Stuff C
Place Site w/in
0.5" of clock
ball(v6)
C38 X18PF
Host Interface
10 SM_MAC#[4..7]
9 SM_MAB#[4..7]
9,10 SM_MAA[0..12]
SM_MD[0..63] 9,10
U7B
RN37 10/8P4R
RN38 10/8P4R
RN36 10/8P4R
9,10 SM_BS0
9,10 SM_BS1
9,10 SM_RAS#
9,10 SM_CAS#
9,10 SM_WE#
6 DCLK_WR
9,10 SM_DQM[0..7]
VCC3SBY
PR9 40.2,1%
C36 22PF
82815 GMCH
SYSTEM MEMORY
9 SM_CKE[0..3]
10 SM_CKE[4..5]
9 SM_CSA#[0..3]
10 SM_CSA#[4..5]
9 SM_CSB#[0..3]
10 SM_CSB#[4..5]
VCC3SBY
BC188 X0.1UF
BC190 X0.1UF
BC191 X0.1UF
BC189 X0.1UF
Backside decouping , should be placed under chipset memory signal field
VDDQ
BC192 X0.1UF
BC193 X0.1UF
BC194 X0.1UF
BC195 X0.1UF
Backside decouping , should be placed under chipset AGP signal field
SM_MAA12
R349 10k
Q30 2N7002
4,6,26 TUAL5
SM_WE# R90 8.2K R_BSEL#0 29
SM_CAS# R89 8.2K R_REFCLK 29
SM_MAA9 R88 10K
R68 X10K SM_MAA10
R77 X10K SM_RAS#
SM_WE# Host Freq : HI=100 LO=66
SM_MAA9 FSB P-MOS Kicker : HI=NON-Cu LO=Cu
SM_CAS# Host Freq : HI=133 LO=100/66
SBA7 LM FREQ : HI=133 LO=100
SM_BS0
SM_BS1 SM/LM muxing strap , active low
SM_MAA10 ALLZ : LO=ALLZ HI=Normal
SM_MAA11 IOQ depth : HI=4 LO=1
SM_MAA12 LO = Future 0.13u Socket 370 processors
HI = Pentium(R) III Processor or Intel(R) Celeron(tm) Processor w/CPUID = 068Xh
SM_RAS# XOR chain : LO=XOR HI=Normal
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U7C
82815 GMCH
Display Cache, Video, and HUB Interface
NOTE : OCLK = 0.5"
RCLK = 1.5"
Do Not Stuff C
Place Site w/in 0.5"
of clock ball(AA21)
Place R as
Close as
possible to
GMCH
Place as close as
Possible to GMCH
and via straight
to VSS plane
Place as close as
Possible to GMCH
and via straight
to VSS plane
U7D
82815 GMCH
Power and Ground
U7E
Solano
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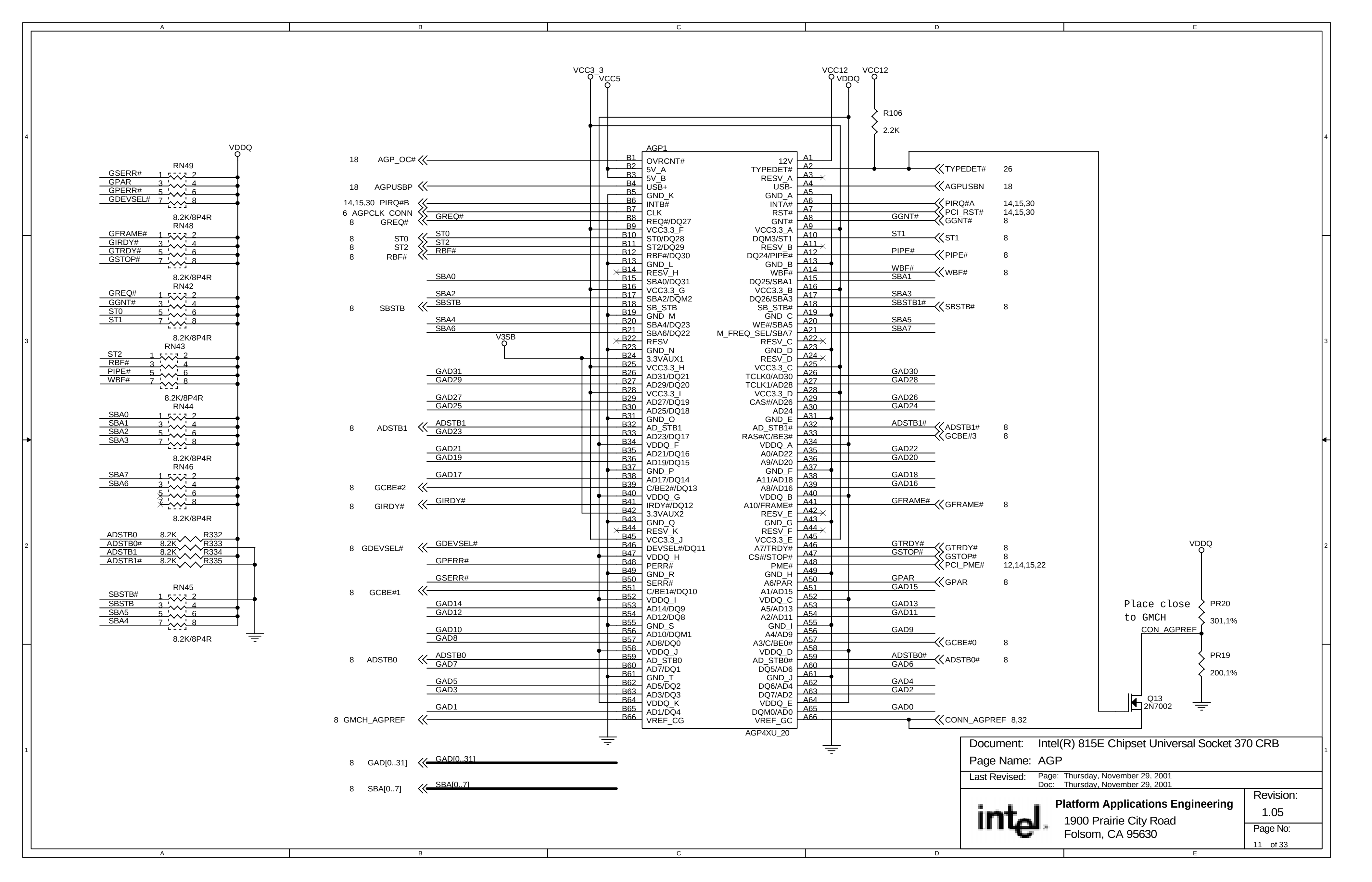


A
B
C
D
E
1
2
3
4
VCC3SBY
DIMM1
DIMM2
DIMM168
SM_MAA[0..12] 7,10
SM_MD[0..63] 7,10
SM_MAB#[4..7] 7
SM_DQM[0..7] 7,10
MEMCLK[0..7] 6
SM_CKE[0..3] 7
SM_CSA#[0..3] 7
SM_CSB#[0..3] 7
SM_WE# 7,10
SM_RAS# 7,10
SM_CAS# 7,10
SM_BS0 7,10
SM_BS1 7,10
SMBDATA 10,13,21,24,30,32
SMBCLK 10,13,21,24,30,32
R28
2.2K
DM_SA_PU 10
Document: Intel(R) 815E Chipset Universal Socket 370 CRB
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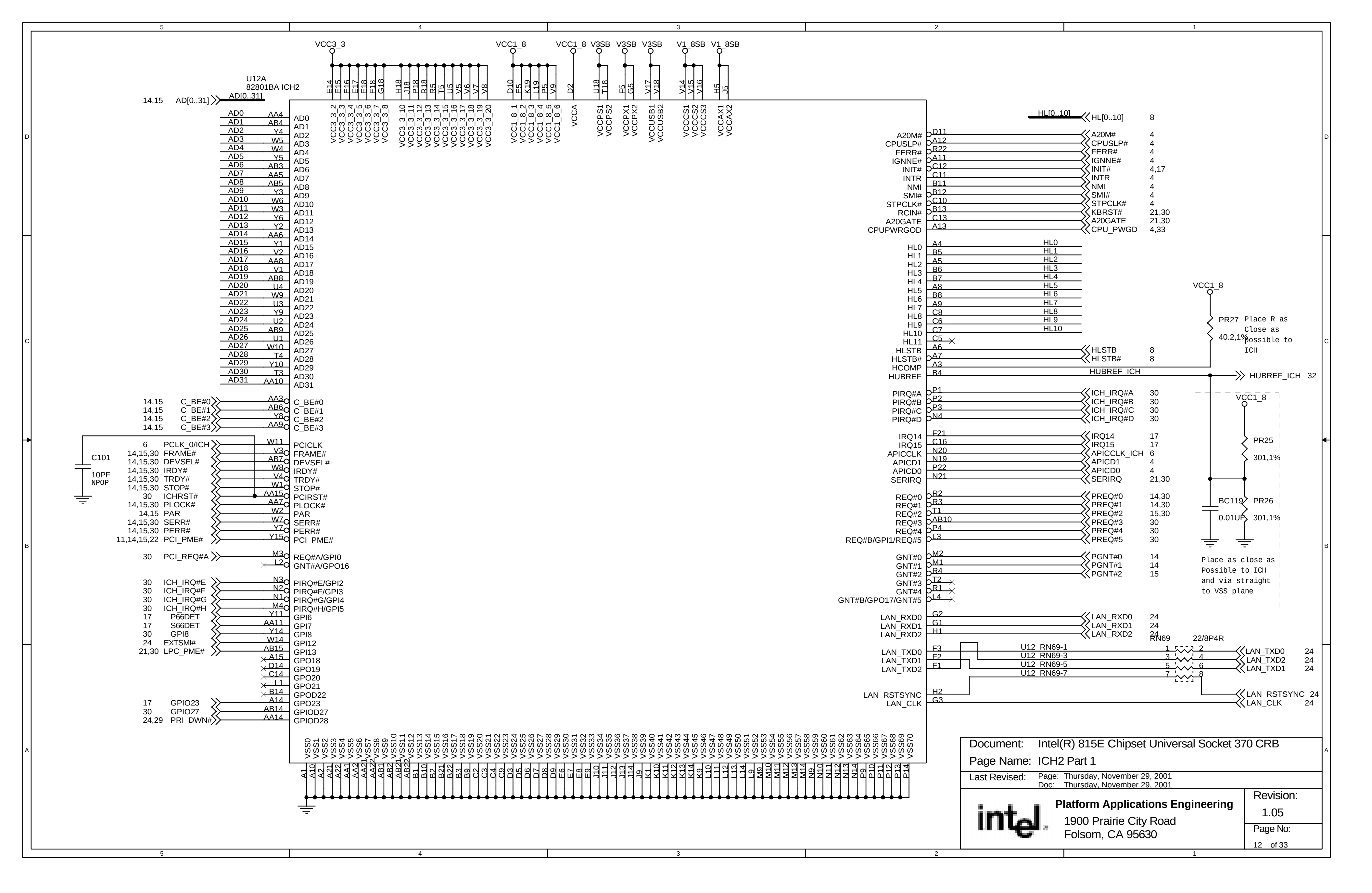


A B C D E
4 3 2 1
VCC3SBY
VCC3SBY
DIMM3
DIMM168
7,9 SM_MAA[0..12] SM_MAA[0..12]
7,9 SM_MD[0..63] SM_MD[0..63]
7 SM_MAC#[4..7] SM_MAC#[4..7]
7,9 SM_DQM[0..7] SM_DQM[0..7]
6 MEMCLK[8..11] MEMCLK[8..11]
7 SM_CKE[4..5] SM_CKE[4..5]
7 SM_CSA#[4..5] SM_CSA#[4..5]
7 SM_CSB#[4..5] SM_CSB#[4..5]
7,9 SM_WE# SM_WE#
7,9 SM_RAS# SM_RAS#
7,9 SM_CAS# SM_CAS#
7,9 SM_BS0 SM_BS0
7,9 SM_BS1 SM_BS1
9,13,21,24,30,32 SMBDATA SMBDATA
9,13,21,24,30,32 SMBCLK SMBCLK
9 DM_SA_PU
1 VSS
SM_MD0 2 DQ0
SM_MD1 3 DQ1
SM_MD2 4 DQ2
SM_MD3 5 DQ3
6 VDD
SM_MD4 7 DQ4
SM_MD5 8 DQ5
SM_MD6 9 DQ6
SM_MD7 10 DQ7
SM_MD8 11 DQ8
12 VSS
SM_MD9 13 DQ9
SM_MD10 14 DQ10
SM_MD11 15 DQ11
SM_MD12 16 DQ12
SM_MD13 17 DQ13
18 VDD
SM_MD14 19 DQ14
SM_MD15 20 DQ15
21 CB0
22 CB1
23 VSS
24 CB8
25 CB9
26 VDD
SM_WE# 27 WE#/WE0#
SM_DQM0 28 DQM0
SM_DQM1 29 DQM1
SM_CSA#4 30 CS0#
31 DU/OE0#
32 VSS
SM_MAA0 33 A0
SM_MAA2 34 A2
SM_MAC#4 35 A4
SM_MAC#6 36 A6
SM_MAA8 37 A8
SM_MAA10 38 A10/AP
SM_BS1 39 BA1/A12
40 VDD
41 VDD
MEMCLK8 42 CLK0/DU
43 VSS
44 DU/OE2#
SM_CSB#4 45 CS2#
SM_DQM2 46 DQM2
SM_DQM3 47 DQM3
48 DU/WE2#
49 VDD
50 CB10
51 CB11
52 CB2
53 CB3
54 VSS
SM_MD16 55 DQ16
SM_MD17 56 DQ17
SM_MD18 57 DQ18
SM_MD19 58 DQ19
59 VDD
SM_MD20 60 DQ20
61 NC
62 VREF/DU
SM_CKE5 63 CKE1
64 VSS
SM_MD21 65 DQ21
SM_MD22 66 DQ22
SM_MD23 67 DQ23
68 VSS
SM_MD24 69 DQ24
SM_MD25 70 DQ25
SM_MD26 71 DQ26
SM_MD27 72 DQ27
73 VDD
SM_MD28 74 DQ28
SM_MD29 75 DQ29
SM_MD30 76 DQ30
SM_MD31 77 DQ31
78 VSS
MEMCLK10 79 CLK2/NC
80 NC
81 WP
SMBDATA 82 SDA
SMBCLK 83 SCL
84 VDD
VSS 85
DQ32 86 SM_MD32
DQ33 87 SM_MD33
DQ34 88 SM_MD34
DQ35 89 SM_MD35
VDD 90
DQ36 91 SM_MD36
DQ37 92 SM_MD37
DQ38 93 SM_MD38
DQ39 94 SM_MD39
DQ40 95 SM_MD40
VSS 96
DQ41 97 SM_MD41
DQ42 98 SM_MD42
DQ43 99 SM_MD43
DQ44 100 SM_MD44
DQ45 101 SM_MD45
VDD 102
DQ46 103 SM_MD46
DQ47 104 SM_MD47
CB4 105
CB5 106
VSS 107
CB12 108
CB13 109
VDD 110
CAS#/DU 111 SM_CAS#
DQM4 112 SM_DQM4
DQM5 113 SM_DQM5
CS1# 114 SM_CSA#5
RAS#/DU 115 SM_RAS#
VSS 116
A1 117 SM_MAA1
A3 118 SM_MAA3
A5 119 SM_MAC#5
A7 120 SM_MAC#7
A9 121 SM_MAA9
BA0/A11 122 SM_BS0
A11/A13 123 SM_MAA11
VDD 124
CLK1/DU 125 MEMCLK9
A12/DU 126 SM_MAA12
VSS 127
CKE0/DU 128 SM_CKE4
CS3# 129 SM_CSB#5
DQM6 130 SM_DQM6
DQM7 131 SM_DQM7
A13/DU 132
VDD 133
CB14 134
CB15 135
CB6 136
CB7 137
VSS 138
DQ48 139 SM_MD48
DQ49 140 SM_MD49
DQ50 141 SM_MD50
DQ51 142 SM_MD51
VDD 143
DQ52 144 SM_MD52
NC 145
VREF/DU 146
REGE 147
VSS 148
DQ53 149 SM_MD53
DQ54 150 SM_MD54
DQ55 151 SM_MD55
VSS 152
DQ56 153 SM_MD56
DQ57 154 SM_MD57
DQ58 155 SM_MD58
DQ59 156 SM_MD59
VDD 157
DQ60 158 SM_MD60
DQ61 159 SM_MD61
DQ62 160 SM_MD62
DQ63 161 SM_MD63
VSS 162
CLK3/NC 163 MEMCLK11
NC 164
SA0 165
SA1 166
SA2 167
VDD 168
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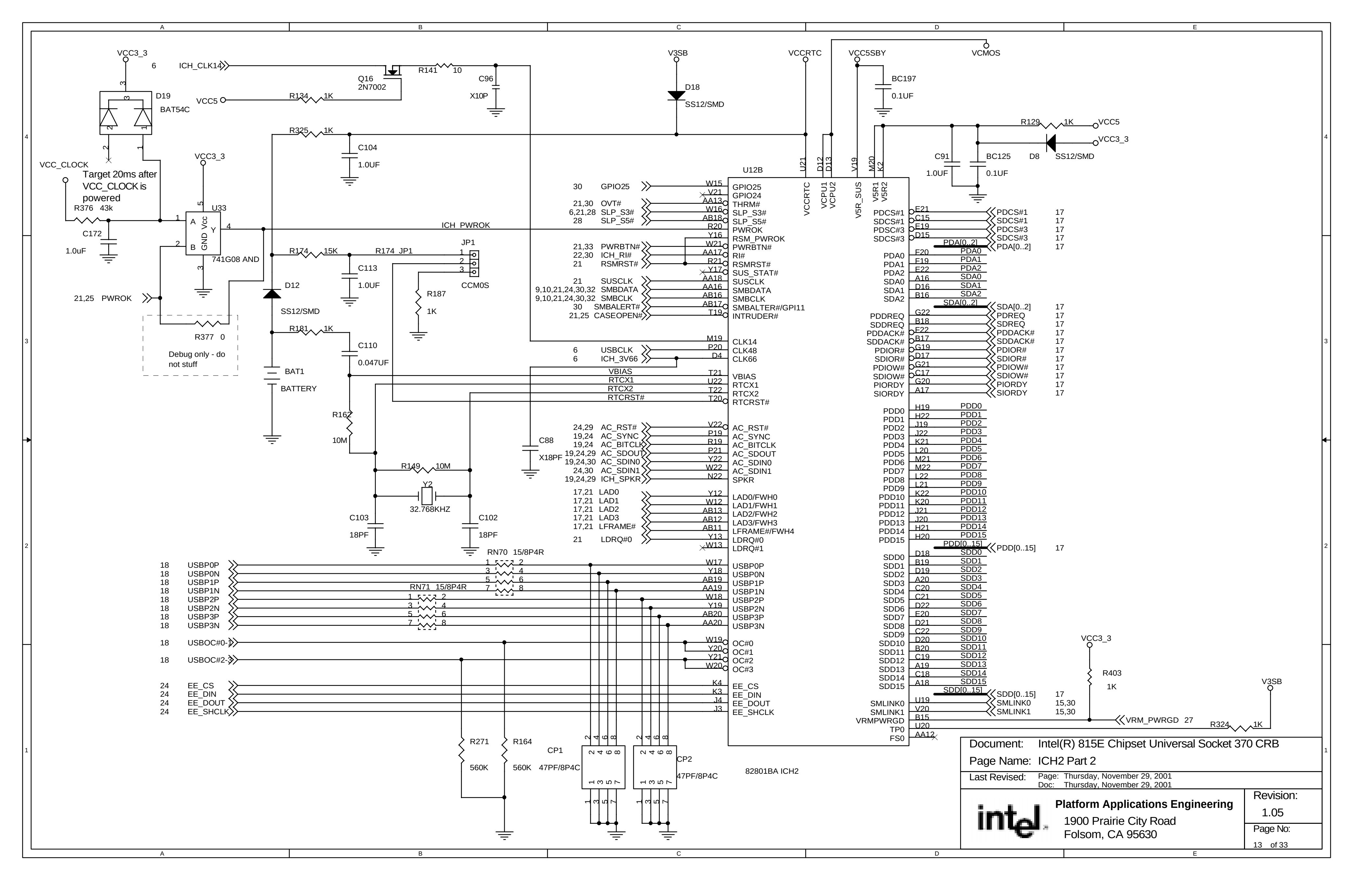


VCC3_3
VCC5
VCC12
VDDQ
VCC12
R106
2.2K
AGP1
AGP4XU_20
VDDQ
RN49
GSERR#
GPAR
GPERR#
GDEVSEL#
8.2K/8P4R
RN48
GFRAME#
GIRDY#
GTRDY#
GSTOP#
8.2K/8P4R
RN42
GREQ#
GGNT#
ST0
ST1
8.2K/8P4R
RN43
ST2
RBF#
PIPE#
WBF#
8.2K/8P4R
RN44
SBA0
SBA1
SBA2
SBA3
8.2K/8P4R
RN46
SBA7
SBA6
8.2K/8P4R
ADSTB0 8.2K R332
ADSTB0# 8.2K R333
ADSTB1 8.2K R334
ADSTB1# 8.2K R335
RN45
SBSTB#
SBSTB
SBA5
SBA4
8.2K/8P4R
18 AGP_OC#
18 AGPUSBP
14,15,30 PIRQ#B
6 AGPCLK_CONN
8 GREQ#
8 ST0
8 ST2
8 RBF#
8 SBSTB
V3SB
8 ADSTB1
8 GCBE#2
8 GIRDY#
8 GDEVSEL#
8 GCBE#1
8 ADSTB0
8 GMCH_AGPREF
8 GAD[0..31]
8 SBA[0..7]
GAD[0..31]
SBA[0..7]
OVRCNT#
5V_A
5V_B
USB+
GND_K
INTB#
CLK
REQ#/DQ27
VCC3.3_F
ST0/DQ28
ST2/DQ29
RBF#/DQ30
GND_L
RESV_H
SBA0/DQ31
VCC3.3_G
SBA2/DQM2
SB_STB
GND_M
SBA4/DQ23
SBA6/DQ22
RESV
GND_N
3.3VAUX1
VCC3.3_H
AD31/DQ21
AD29/DQ20
VCC3.3_I
AD27/DQ19
AD25/DQ18
GND_O
AD_STB1
AD23/DQ17
VDDQ_F
AD21/DQ16
AD19/DQ15
GND_P
AD17/DQ14
C/BE2#/DQ13
VDDQ_G
IRDY#/DQ12
3.3VAUX2
GND_Q
RESV_K
VCC3.3_J
DEVSEL#/DQ11
VDDQ_H
PERR#
GND_R
SERR#
C/BE1#/DQ10
VDDQ_I
AD14/DQ9
AD12/DQ8
GND_S
AD10/DQM1
AD8/DQ0
VDDQ_J
AD_STB0
AD7/DQ1
GND_T
AD5/DQ2
AD3/DQ3
VDDQ_K
AD1/DQ4
VREF_CG
12V
TYPEDET#
RESV_A
USB-
GND_A
INTA#
RST#
GNT#
VCC3.3_A
DQM3/ST1
RESV_B
DQ24/PIPE#
GND_B
WBF#
DQ25/SBA1
VCC3.3_B
DQ26/SBA3
SB_STB#
GND_C
WE#/SBA5
M_FREQ_SEL/SBA7
RESV_C
GND_D
RESV_D
VCC3.3_C
TCLK0/AD30
TCLK1/AD28
VCC3.3_D
CAS#/AD26
AD24
GND_E
AD_STB1#
RAS#/C/BE3#
VDDQ_A
A0/AD22
A9/AD20
GND_F
A11/AD18
A8/AD16
VDDQ_B
A10/FRAME#
RESV_E
GND_G
RESV_F
VCC3.3_E
A7/TRDY#
CS#/STOP#
PME#
GND_H
A6/PAR
A1/AD15
VDDQ_C
A5/AD13
A2/AD11
GND_I
A4/AD9
A3/C/BE0#
VDDQ_D
AD_STB0#
DQ5/AD6
GND_J
DQ6/AD4
DQ7/AD2
VDDQ_E
DQM0/AD0
VREF_GC
TYPEDET# 26
AGPUSBN 18
PIRQ#A 14,15,30
PCI_RST# 14,15,30
GGNT# 8
ST1 8
PIPE# 8
WBF# 8
SBSTB# 8
ADSTB1# 8
GCBE#3 8
GFRAME# 8
GTRDY# 8
GSTOP# 8
PCI_PME# 12,14,15,22
GPAR 8
GCBE#0 8
ADSTB0# 8
CONN_AGPREF 8,32
VDDQ
Place close
to GMCH
PR20
301,1%
CON_AGPREF
PR19
200,1%
Q13
2N7002
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CH6-18

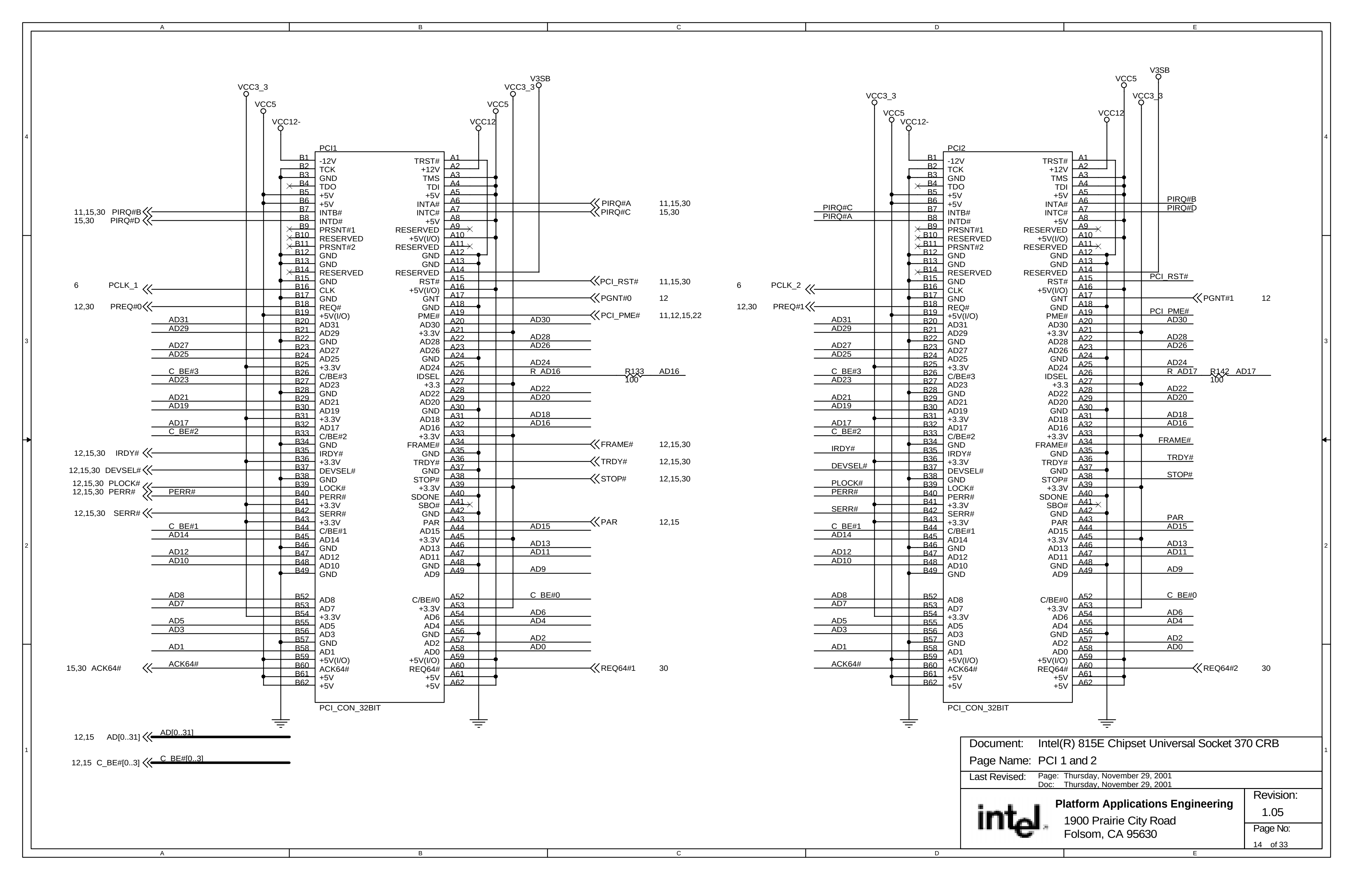


U12A
82801BA ICH2
14,15 AD[0..31]
AD[0..31]
AD0 AA4 AD0
AD1 AB4 AD1
AD2 Y4 AD2
AD3 W5 AD3
AD4 W4 AD4
AD5 Y5 AD5
AD6 AB3 AD6
AD7 AA5 AD7
AD8 AB5 AD8
AD9 Y3 AD9
AD10 W6 AD10
AD11 W3 AD11
AD12 Y6 AD12
AD13 Y2 AD13
AD14 AA6 AD14
AD15 Y1 AD15
AD16 V2 AD16
AD17 AA8 AD17
AD18 V1 AD18
AD19 AB8 AD19
AD20 U4 AD20
AD21 W9 AD21
AD22 U3 AD22
AD23 Y9 AD23
AD24 U2 AD24
AD25 AB9 AD25
AD26 U1 AD26
AD27 W10 AD27
AD28 T4 AD28
AD29 Y10 AD29
AD30 T3 AD30
AD31 AA10 AD31
14,15 C_BE#0 AA3 C_BE#0
14,15 C_BE#1 AB6 C_BE#1
14,15 C_BE#2 Y8 C_BE#2
14,15 C_BE#3 AA9 C_BE#3
C101
10PF
NPOP
6 PCLK_0/ICH W11 PCICLK
14,15,30 FRAME# V3 FRAME#
14,15,30 DEVSEL# AB7 DEVSEL#
14,15,30 IRDY# W8 IRDY#
14,15,30 TRDY# V4 TRDY#
14,15,30 STOP# W1 STOP#
30 ICHRST# AA15 PCIRST#
14,15,30 PLOCK# AA7 PLOCK#
14,15 PAR W2 PAR
14,15,30 SERR# W7 SERR#
14,15,30 PERR# Y7 PERR#
11,14,15,22 PCI_PME# Y15 PCI_PME#
30 PCI_REQ#A M3 REQ#A/GPI0
L2 GNT#A/GPO16
30 ICH_IRQ#E N3 PIRQ#E/GPI2
30 ICH_IRQ#F N2 PIRQ#F/GPI3
30 ICH_IRQ#G N1 PIRQ#G/GPI4
30 ICH_IRQ#H M4 PIRQ#H/GPI5
17 P66DET Y11 GPI6
17 S66DET AA11 GPI7
30 GPI8 Y14 GPI8
24 EXTSMI# W14 GPI12
21,30 LPC_PME# AB15 GPI13
A15 GPO18
D14 GPO19
C14 GPO20
L1 GPO21
B14 GPOD22
17 GPIO23 A14 GPO23
30 GPIO27 AB14 GPIOD27
24,29 PRI_DWN# AA14 GPIOD28
VCC3_3
E14 E15 E16 E17 E18 F18 G18 H18 J18 P18 R18 R5 T5 U5 V5 V6 V7 V8
VCC3_3_2 VCC3_3_3 VCC3_3_4 VCC3_3_5 VCC3_3_6 VCC3_3_7 VCC3_3_8 VCC3_3_10 VCC3_3_11 VCC3_3_12 VCC3_3_13 VCC3_3_14 VCC3_3_15 VCC3_3_16 VCC3_3_17 VCC3_3_18 VCC3_3_19 VCC3_3_20
VCC1_8
D10 E5 K19 L19 P5 V9
VCC1_8_1 VCC1_8_2 VCC1_8_3 VCC1_8_4 VCC1_8_5 VCC1_8_6
VCC1_8 D2 VCCA
V3SB U18 T18 VCCPS1 VCCPS2
V3SB F5 G5 VCCPX1 VCCPX2
V3SB V17 V18 VCCUSB1 VCCUSB2
V1_8SB V14 V15 V16 VCCCS1 VCCCS2 VCCCS3
V1_8SB H5 J5 VCCAX1 VCCAX2
HL[0..10] HL[0..10] 8
A20M# D11 A20M# 4
CPUSLP# A12 CPUSLP# 4
FERR# R22 FERR# 4
IGNNE# A11 IGNNE# 4
INIT# C12 INIT# 4,17
INTR C11 INTR 4
NMI B11 NMI 4
SMI# B12 SMI# 4
STPCLK# C10 STPCLK# 4
RCIN# B13 KBRST# 21,30
A20GATE C13 A20GATE 21,30
CPUPWRGOD A13 CPU_PWGD 4,33
HL0 A4 HL0
HL1 B5 HL1
HL2 A5 HL2
HL3 B6 HL3
HL4 B7 HL4
HL5 A8 HL5
HL6 B8 HL6
HL7 A9 HL7
HL8 C8 HL8
HL9 C6 HL9
HL10 C7 HL10
HL11 C5
HLSTB A6 HLSTB 8
HLSTB# A7 HLSTB# 8
HCOMP A3
HUBREF B4 HUBREF_ICH
HUBREF_ICH 32
VCC1_8
PR27 40.2,1%
Place R as Close as possible to ICH
PIRQ#A P1 ICH_IRQ#A 30
PIRQ#B P2 ICH_IRQ#B 30
PIRQ#C P3 ICH_IRQ#C 30
PIRQ#D N4 ICH_IRQ#D 30
IRQ14 F21 IRQ14 17
IRQ15 C16 IRQ15 17
APICCLK N20 APICCLK_ICH 6
APICD1 N19 APICD1 4
APICD0 P22 APICD0 4
SERIRQ N21 SERIRQ 21,30
REQ#0 R2 PREQ#0 14,30
REQ#1 R3 PREQ#1 14,30
REQ#2 T1 PREQ#2 15,30
REQ#3 AB10 PREQ#3 30
REQ#4 P4 PREQ#4 30
REQ#B/GPI1/REQ#5 L3 PREQ#5 30
GNT#0 M2 PGNT#0 14
GNT#1 M1 PGNT#1 14
GNT#2 R4 PGNT#2 15
GNT#3 T2
GNT#4 R1
GNT#B/GPO17/GNT#5 L4
VCC1_8
PR25 301,1%
BC119 0.01UF
PR26 301,1%
Place as close as Possible to ICH and via straight to VSS plane
LAN_RXD0 G2 LAN_RXD0 24
LAN_RXD1 G1 LAN_RXD1 24
LAN_RXD2 H1 LAN_RXD2 24
RN69 22/8P4R
LAN_TXD0 F3 U12_RN69-1
LAN_TXD1 F2 U12_RN69-3
LAN_TXD2 F1 U12_RN69-5
U12_RN69-7
LAN_TXD0 24
LAN_TXD2 24
LAN_TXD1 24
LAN_RSTSYNC H2 LAN_RSTSYNC 24
LAN_CLK G3 LAN_CLK 24
VSS0 ... VSS70
A1 A10 A2 A21 A22 AA1 AA2 AA21 AA22 AB1 AB2 AB21 AB22 B1 B10 B2 B21 B22 B3 B9 C2 C3 C4 C9 D3 D4 D5 D6 D7 D8 D9 E6 E7 E8 E9 J10 J11 J12 J13 J14 J9 K1 K10 K11 K12 K13 K14 K9 L10 L11 L12 L13 L14 L9 M9 M10 M11 M12 M13 M14 N9 N10 N11 N12 N13 N14 P9 P10 P11 P12 P13 P14
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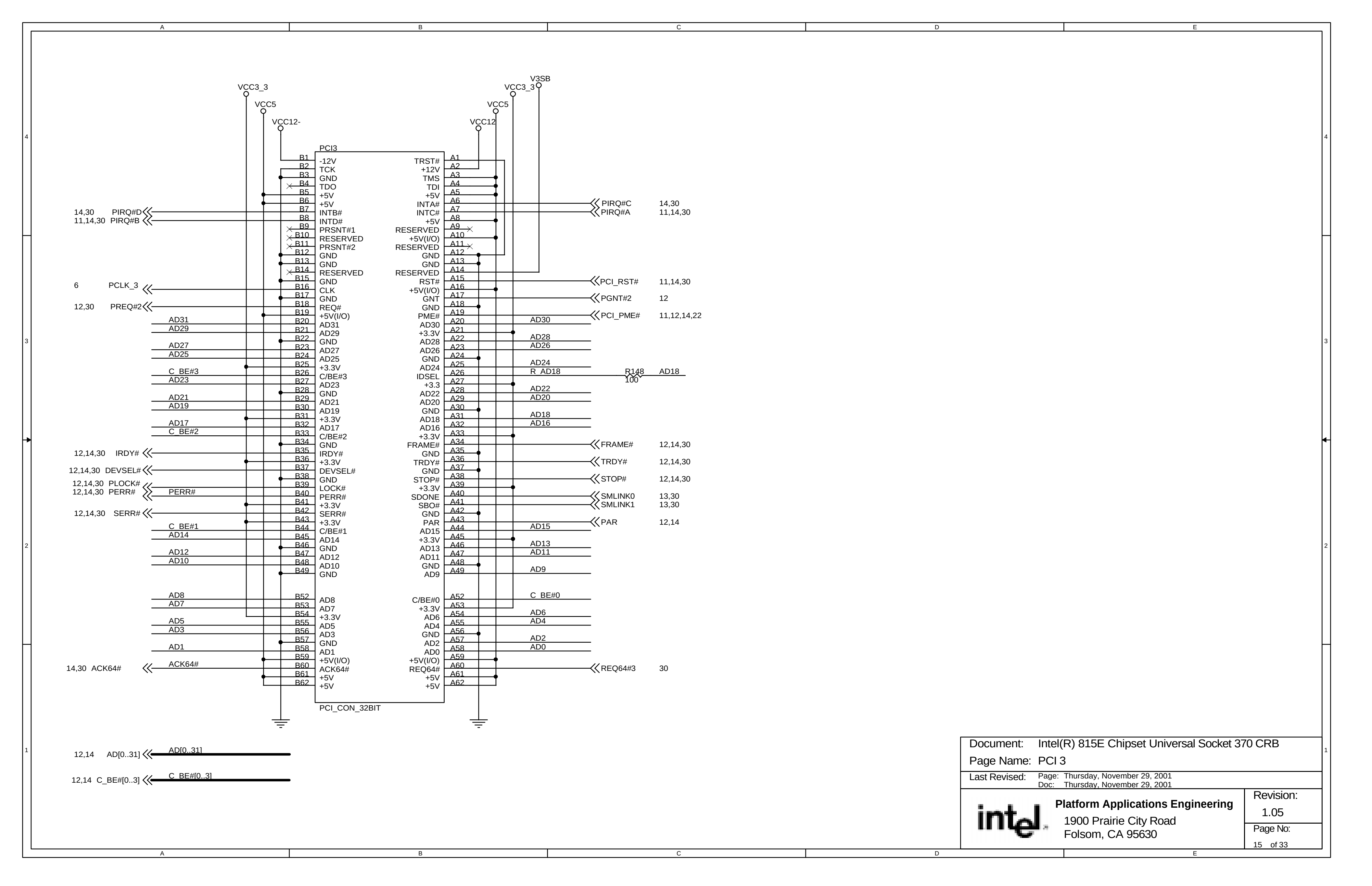


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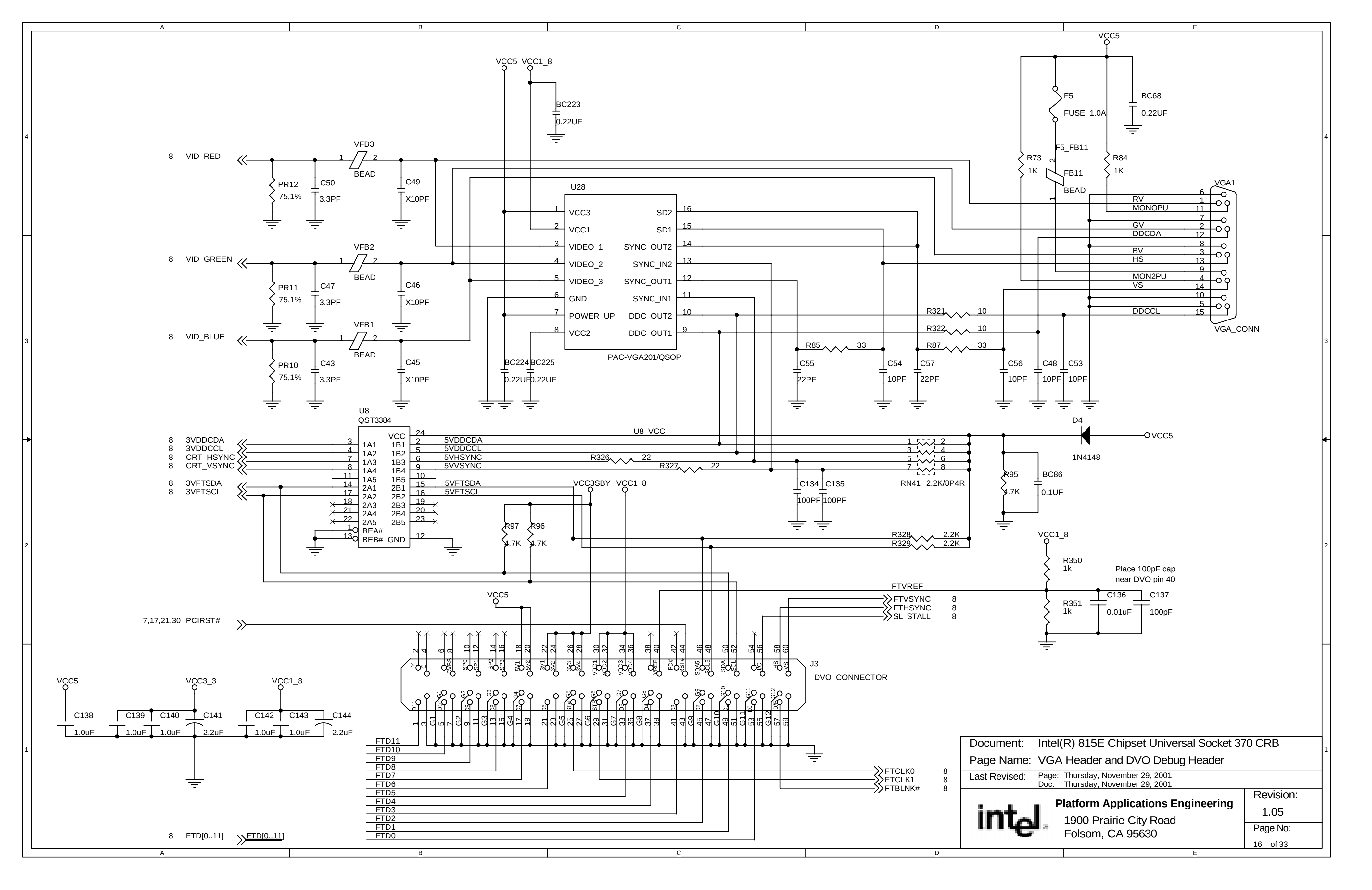
PCI1
PCI_CON_32BIT
PCI2
PCI_CON_32BIT
VCC3_3
VCC5
VCC12-
VCC12
V3SB
11,15,30 PIRQ#B
15,30 PIRQ#D
PIRQ#A 11,15,30
PIRQ#C 15,30
6 PCLK_1
12,30 PREQ#0
PCI_RST# 11,15,30
PGNT#0 12
PCI_PME# 11,12,15,22
R133 100 AD16
12,15,30 IRDY#
12,15,30 DEVSEL#
12,15,30 PLOCK#
12,15,30 PERR#
12,15,30 SERR#
FRAME# 12,15,30
TRDY# 12,15,30
STOP# 12,15,30
PAR 12,15
15,30 ACK64#
REQ64#1 30
12,15 AD[0..31]
12,15 C_BE#[0..3]
6 PCLK_2
12,30 PREQ#1
PGNT#1 12
R142 100 AD17
REQ64#2 30
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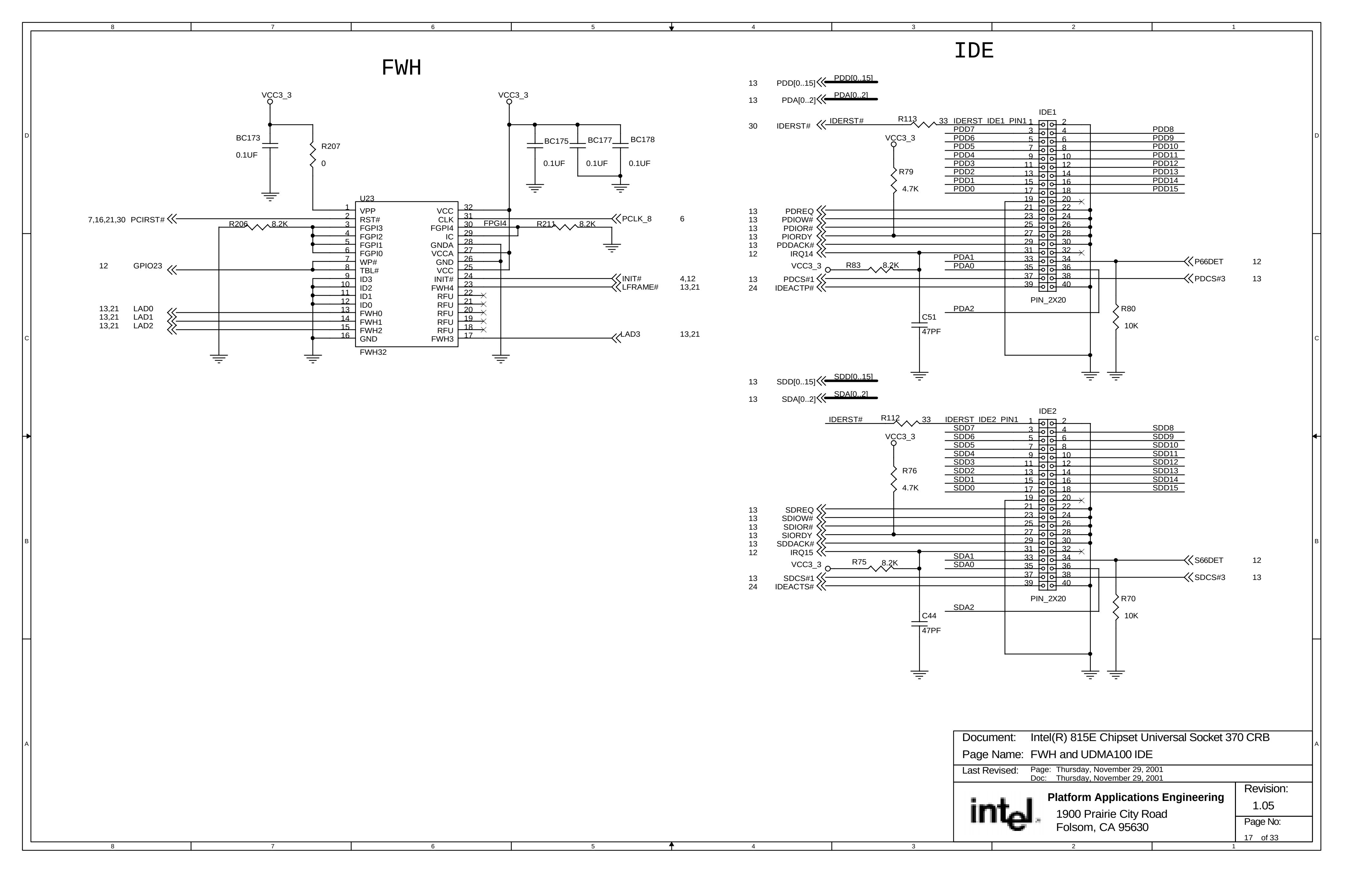


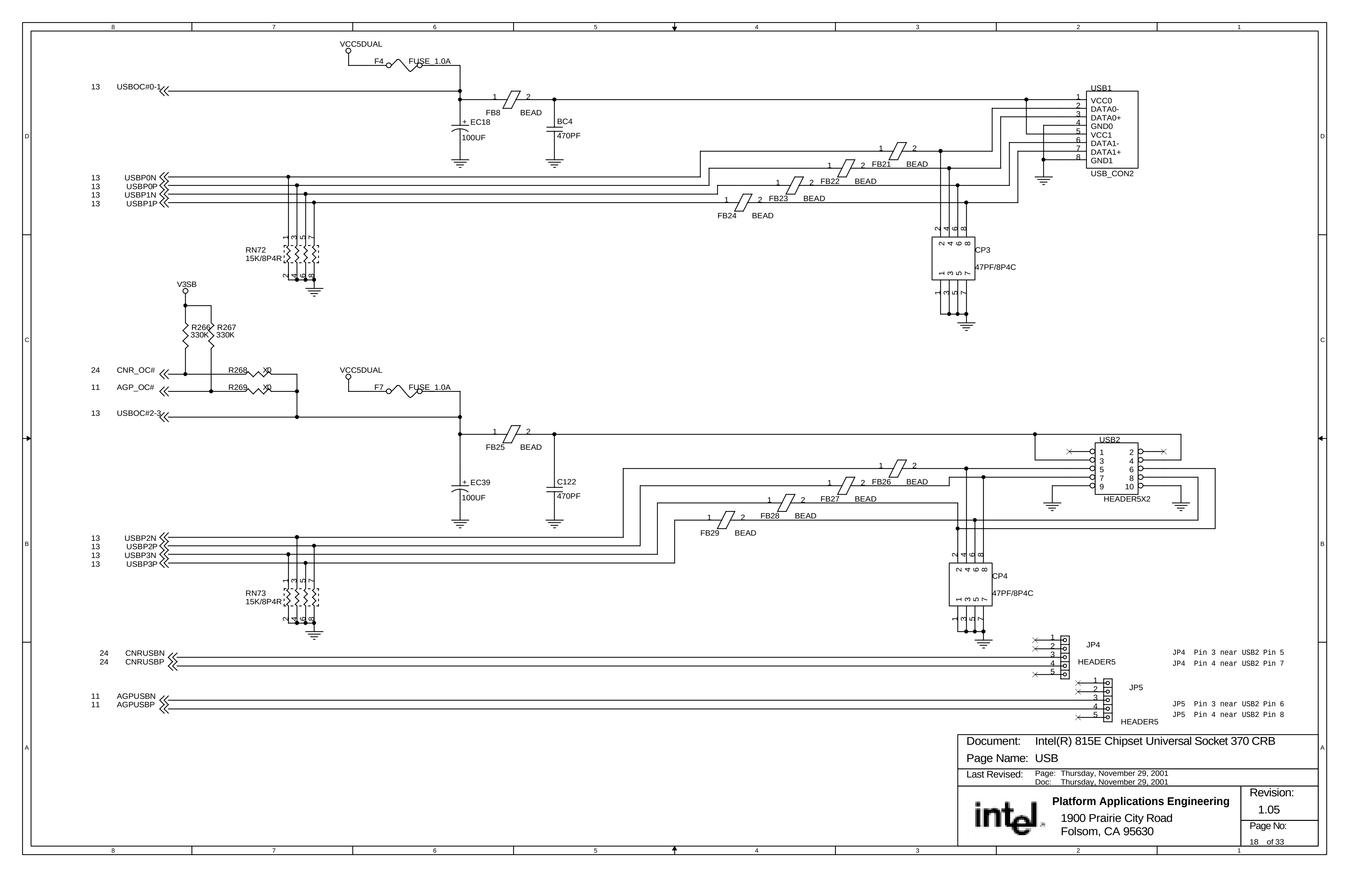
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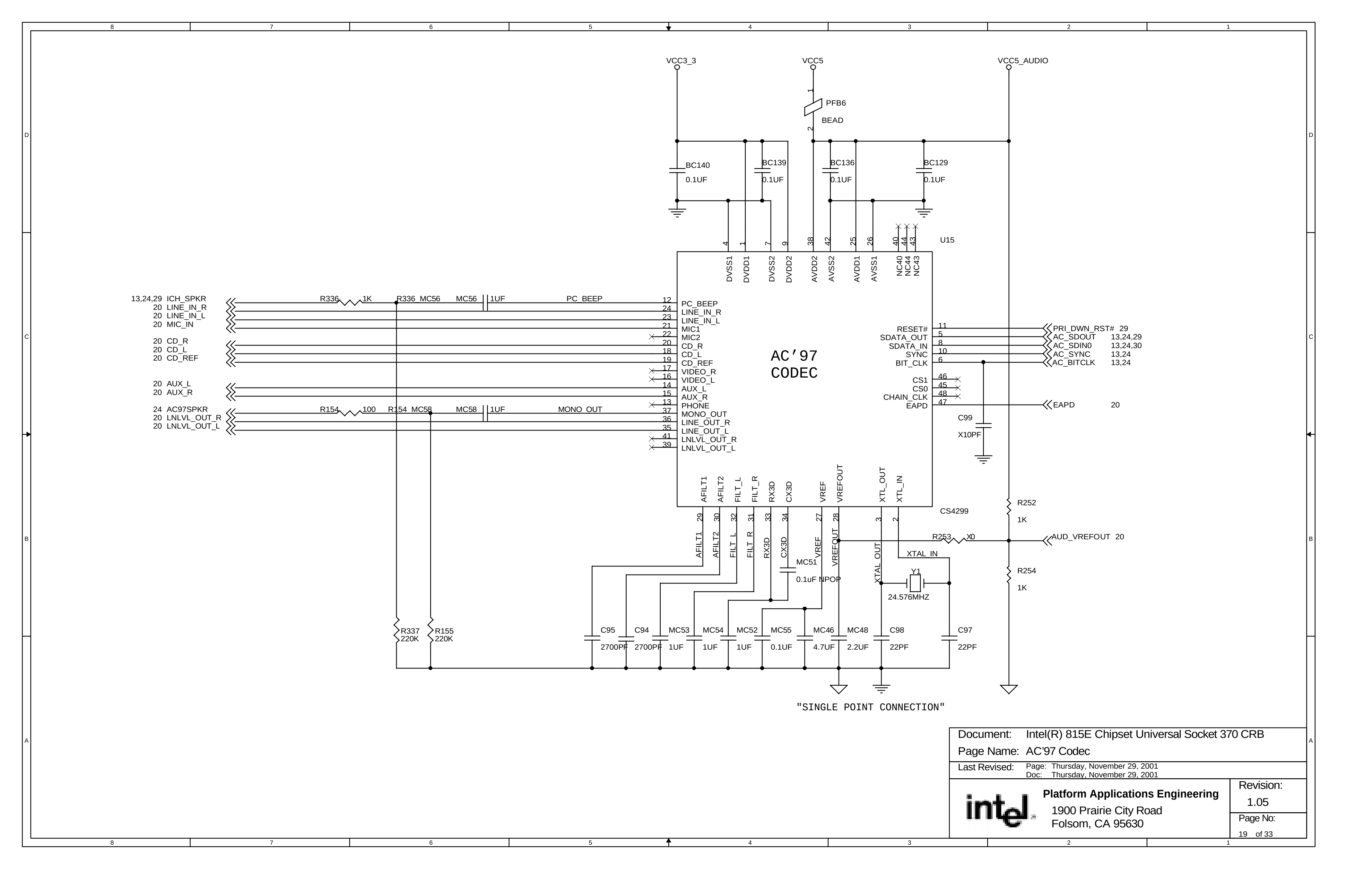
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VID_RED
VID_GREEN
VID_BLUE
VFB3
VFB2
VFB1
BEAD
PR12
PR11
PR10
75,1%
C50
C47
C43
3.3PF
C49
C46
C45
X10PF
U28
VCC3
VCC1
VIDEO_1
VIDEO_2
VIDEO_3
GND
POWER_UP
VCC2
SD2
SD1
SYNC_OUT2
SYNC_IN2
SYNC_OUT1
SYNC_IN1
DDC_OUT2
DDC_OUT1
PAC-VGA201/QSOP
BC223
BC224
BC225
0.22UF
VCC5
VCC1_8
F5
FUSE_1.0A
F5_FB11
FB11
BC68
R73
R84
1K
VGA1
VGA_CONN
RV
MONOPU
GV
DDCDA
BV
HS
MON2PU
VS
DDCCL
R321
R322
R85
R87
C55
C54
C57
C56
C48
C53
22PF
10PF
U8
QST3384
3VDDCDA
3VDDCCL
CRT_HSYNC
CRT_VSYNC
3VFTSDA
3VFTSCL
5VDDCDA
5VDDCCL
5VHSYNC
5VVSYNC
5VFTSDA
5VFTSCL
BEA#
BEB#
U8_VCC
R326
R327
C134
C135
100PF
RN41 2.2K/8P4R
D4
1N4148
R95
4.7K
BC86
0.1UF
VCC3SBY
R97
R96
R328
R329
2.2K
R350
R351
1k
Place 100pF cap
near DVO pin 40
C136
0.01uF
C137
100pF
FTVREF
FTVSYNC
FTHSYNC
SL_STALL
PCIRST#
J3
DVO CONNECTOR
VCC3_3
C138
C139
C140
C141
C142
C143
C144
1.0uF
2.2uF
FTD11
FTD10
FTD9
FTD8
FTD7
FTD6
FTD5
FTD4
FTD3
FTD2
FTD1
FTD0
FTCLK0
FTCLK1
FTBLNK#
FTD[0..11]
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FWH
IDE
VCC3_3
BC173
0.1UF
R207
0
BC175
BC177
BC178
0.1UF
U23
VPP
RST#
FGPI3
FGPI2
FGPI1
FGPI0
WP#
TBL#
ID3
ID2
ID1
ID0
FWH0
FWH1
FWH2
GND
VCC
CLK
FGPI4
IC
GNDA
VCCA
GND
VCC
INIT#
FWH4
RFU
FWH3
FWH32
7,16,21,30 PCIRST#
R206 8.2K
12 GPIO23
13,21 LAD0
13,21 LAD1
13,21 LAD2
FPGI4
R211 8.2K
PCLK_8 6
INIT# 4,12
LFRAME# 13,21
LAD3 13,21
13 PDD[0..15]
13 PDA[0..2]
30 IDERST#
R113 33
IDERST_IDE1_PIN1
IDE1
PDD7 PDD6 PDD5 PDD4 PDD3 PDD2 PDD1 PDD0
PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15
R79
4.7K
13 PDREQ
13 PDIOW#
13 PDIOR#
13 PIORDY
13 PDDACK#
12 IRQ14
VCC3_3
R83 8.2K
PDA1
PDA0
P66DET 12
13 PDCS#1
24 IDEACTP#
PDCS#3 13
PIN_2X20
PDA2
C51
47PF
R80
10K
13 SDD[0..15]
13 SDA[0..2]
IDERST#
R112 33
IDERST_IDE2_PIN1
IDE2
SDD7 SDD6 SDD5 SDD4 SDD3 SDD2 SDD1 SDD0
SDD8 SDD9 SDD10 SDD11 SDD12 SDD13 SDD14 SDD15
R76
4.7K
13 SDREQ
13 SDIOW#
13 SDIOR#
13 SIORDY
13 SDDACK#
12 IRQ15
R75 8.2K
SDA1
SDA0
S66DET 12
13 SDCS#1
24 IDEACTS#
SDCS#3 13
PIN_2X20
SDA2
C44
47PF
R70
10K
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VCC5DUAL
F4 FUSE_1.0A
13 USBOC#0-1
FB8 BEAD
EC18 100UF
BC4 470PF
USB1
VCC0
DATA0-
DATA0+
GND0
VCC1
DATA1-
DATA1+
GND1
USB_CON2
13 USBP0N
13 USBP0P
13 USBP1N
13 USBP1P
FB21 BEAD
FB22 BEAD
FB23 BEAD
FB24 BEAD
RN72 15K/8P4R
CP3 47PF/8P4C
V3SB
R266 330K
R267 330K
24 CNR_OC#
11 AGP_OC#
13 USBOC#2-3
R268 X0
R269 X0
VCC5DUAL
F7 FUSE_1.0A
FB25 BEAD
EC39 100UF
C122 470PF
USB2
HEADER5X2
FB26 BEAD
FB27 BEAD
FB28 BEAD
FB29 BEAD
13 USBP2N
13 USBP2P
13 USBP3N
13 USBP3P
RN73 15K/8P4R
CP4 47PF/8P4C
JP4 HEADER5
24 CNRUSBN
24 CNRUSBP
JP4 Pin 3 near USB2 Pin 5
JP4 Pin 4 near USB2 Pin 7
11 AGPUSBN
11 AGPUSBP
JP5 HEADER5
JP5 Pin 3 near USB2 Pin 6
JP5 Pin 4 near USB2 Pin 8
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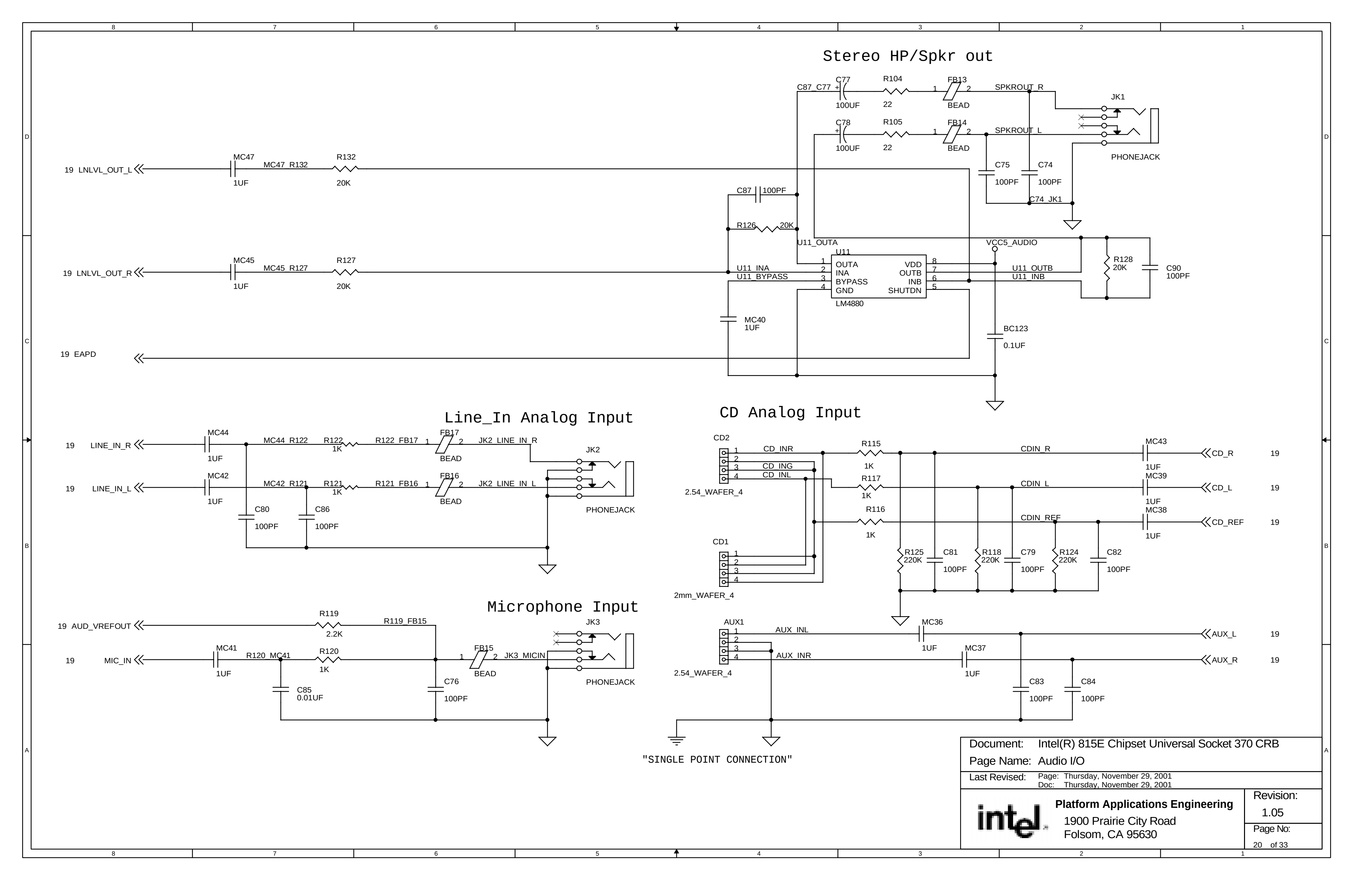
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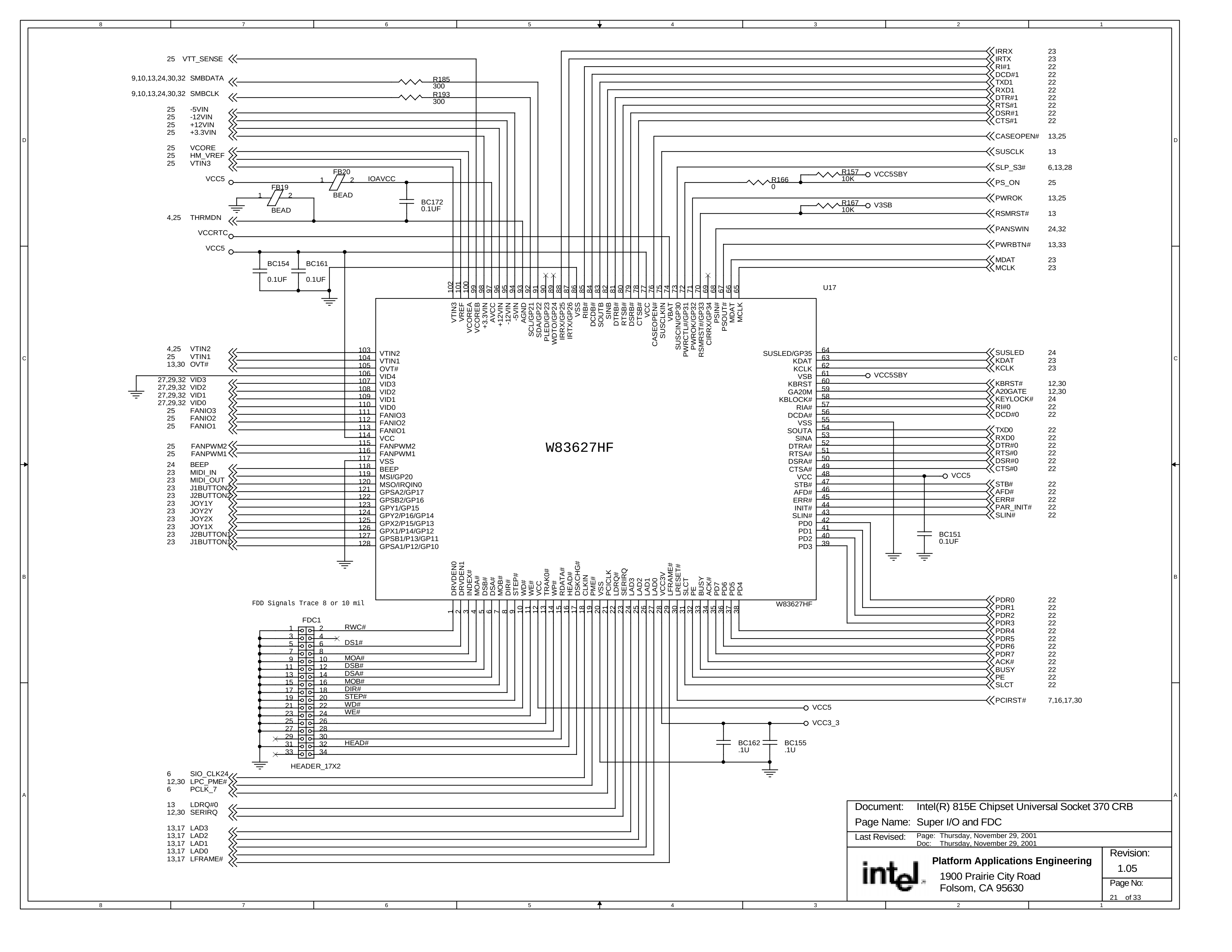
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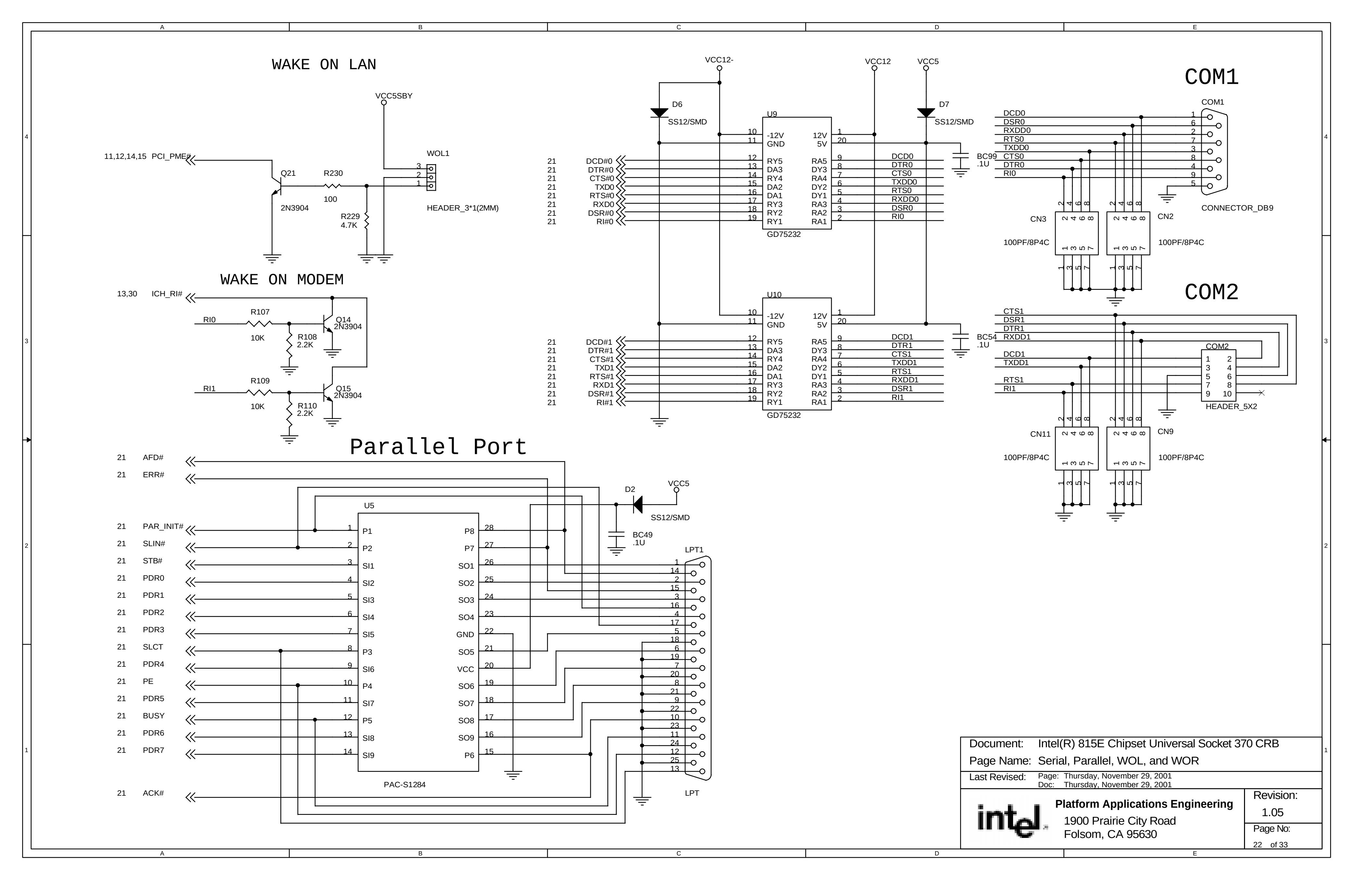
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C87_C77
C77
100UF
R104
22
FB13
BEAD
SPKROUT_R
JK1
C78
100UF
R105
22
FB14
BEAD
SPKROUT_L
PHONEJACK
C75
100PF
C74
100PF
C74_JK1
19 LNLVL_OUT_L
MC47
1UF
MC47_R132
R132
20K
C87
100PF
R126
20K
U11_OUTA
VCC5_AUDIO
U11
OUTA
INA
BYPASS
GND
VDD
OUTB
INB
SHUTDN
LM4880
R128
20K
C90
100PF
U11_OUTB
U11_INB
19 LNLVL_OUT_R
MC45
1UF
MC45_R127
R127
20K
U11_INA
U11_BYPASS
MC40
1UF
BC123
0.1UF
19 EAPD
Line_In Analog Input
19 LINE_IN_R
MC44
1UF
MC44_R122
R122
1K
R122_FB17
FB17
BEAD
JK2_LINE_IN_R
JK2
19 LINE_IN_L
MC42
1UF
MC42_R121
R121
1K
R121_FB16
FB16
BEAD
JK2_LINE_IN_L
C80
100PF
C86
100PF
PHONEJACK
CD Analog Input
CD2
CD_INR
CD_ING
CD_INL
2.54_WAFER_4
R115
1K
R117
1K
R116
1K
CDIN_R
CDIN_L
CDIN_REF
MC43
1UF
CD_R
19
MC39
1UF
CD_L
19
MC38
1UF
CD_REF
19
CD1
2mm_WAFER_4
R125
220K
C81
100PF
R118
220K
C79
100PF
R124
220K
C82
100PF
Microphone Input
19 AUD_VREFOUT
R119
2.2K
R119_FB15
JK3
19 MIC_IN
MC41
1UF
R120_MC41
R120
1K
FB15
BEAD
JK3_MICIN
C85
0.01UF
C76
100PF
PHONEJACK
AUX1
AUX_INL
AUX_INR
2.54_WAFER_4
MC36
1UF
MC37
1UF
AUX_L
19
AUX_R
19
C83
100PF
C84
100PF
"SINGLE POINT CONNECTION"
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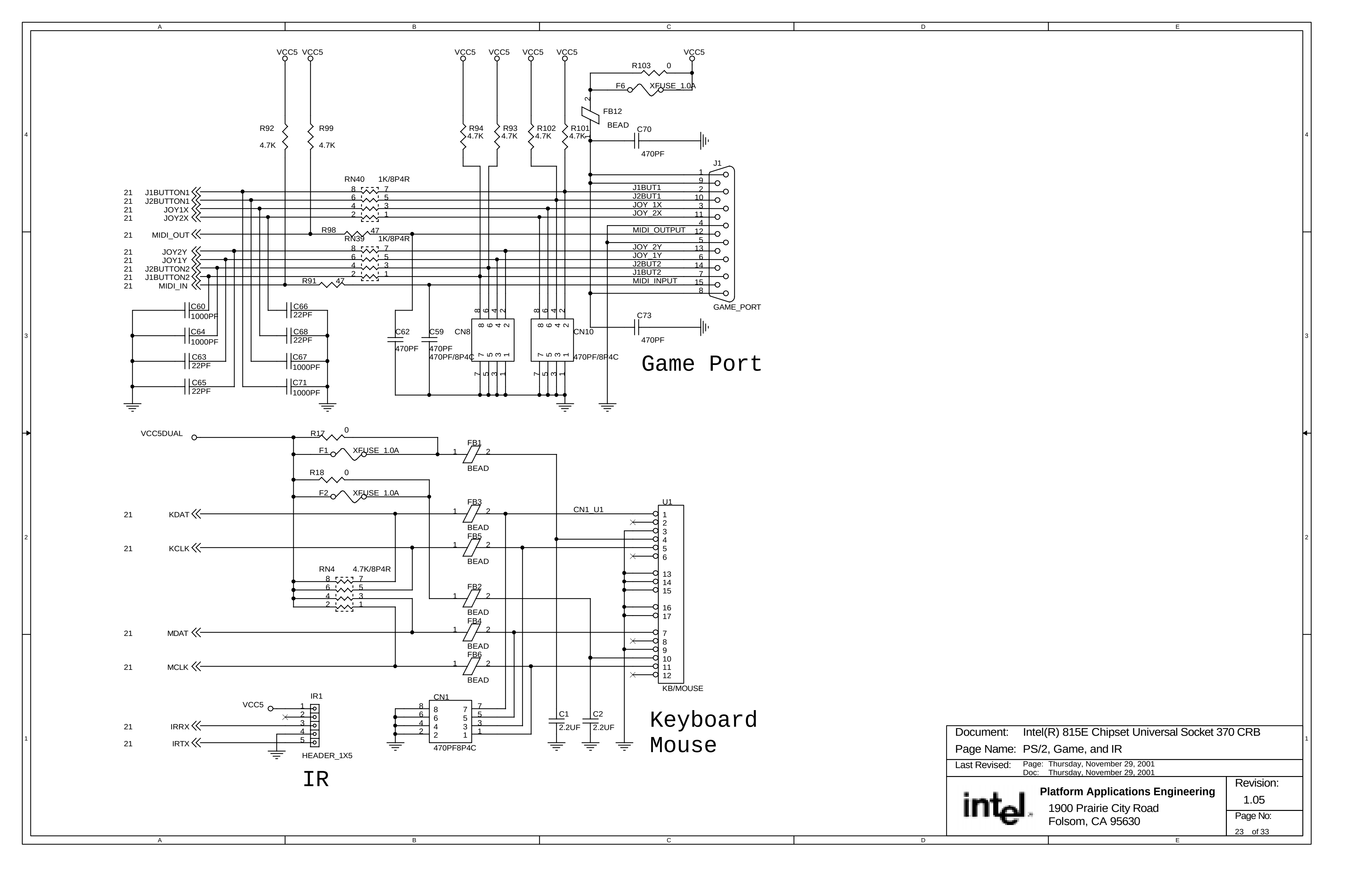
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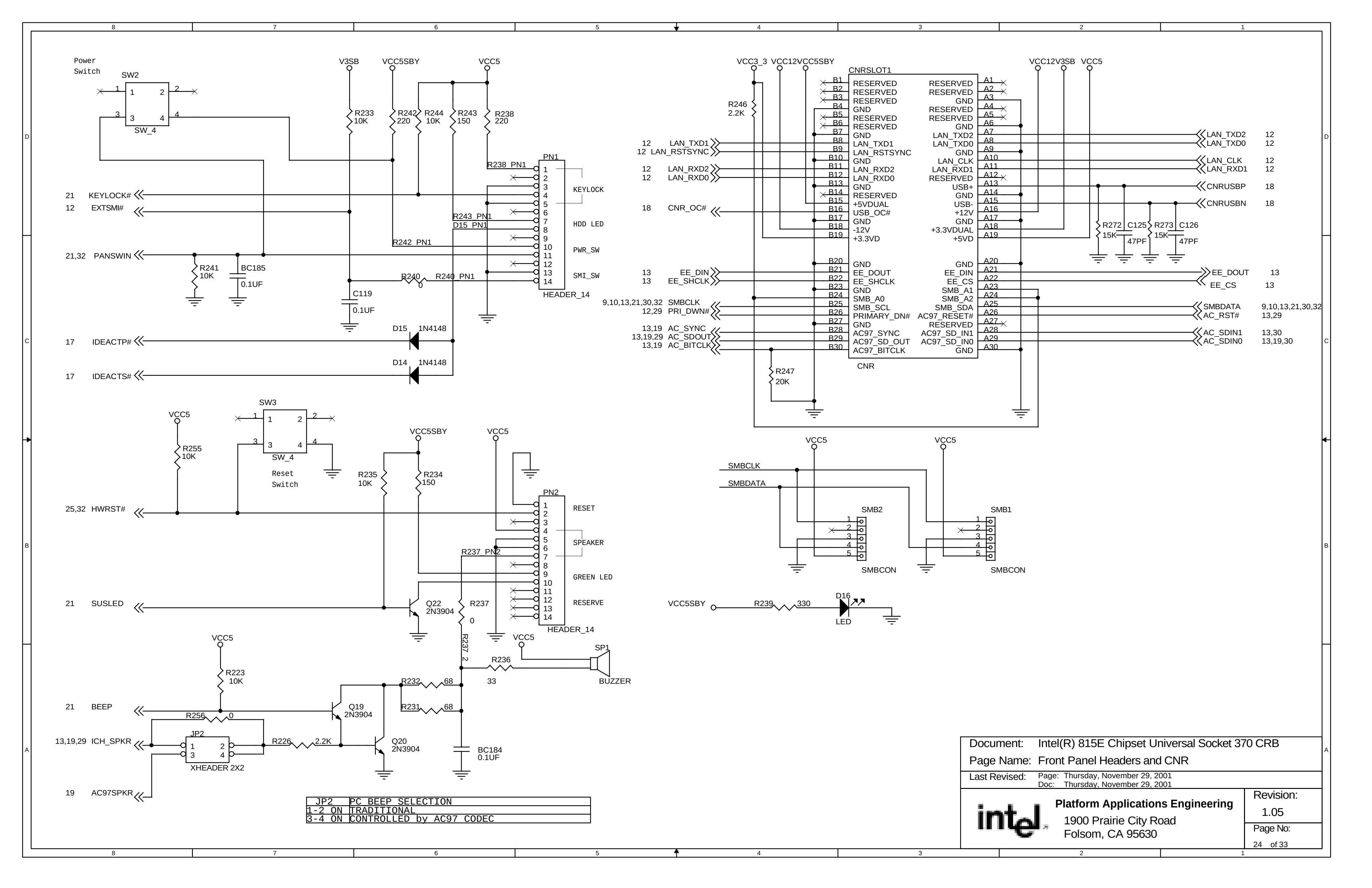
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Game Port
Keyboard Mouse
IR
VCC5
R92 4.7K
R99 4.7K
R94 4.7K
R93 4.7K
R102 4.7K
R101 4.7K
R103 0
F6 XFUSE_1.0A
FB12 BEAD
C70 470PF
C73 470PF
J1
GAME_PORT
RN40 1K/8P4R
RN39 1K/8P4R
R98 47
R91 47
J1BUTTON1
J2BUTTON1
JOY1X
JOY2X
MIDI_OUT
JOY2Y
JOY1Y
J2BUTTON2
J1BUTTON2
MIDI_IN
J1BUT1
J2BUT1
JOY_1X
JOY_2X
MIDI_OUTPUT
JOY_2Y
JOY_1Y
J2BUT2
J1BUT2
MIDI_INPUT
C60 1000PF
C64 1000PF
C63 22PF
C65 22PF
C66 22PF
C68 22PF
C67 1000PF
C71 1000PF
C62 470PF
C59 470PF
CN8 470PF/8P4C
CN10 470PF/8P4C
VCC5DUAL
R17 0
F1 XFUSE_1.0A
R18 0
F2 XFUSE_1.0A
FB1 BEAD
FB3 BEAD
FB5 BEAD
FB2 BEAD
FB4 BEAD
FB6 BEAD
KDAT
KCLK
MDAT
MCLK
RN4 4.7K/8P4R
CN1_U1
U1
KB/MOUSE
CN1 470PF8P4C
C1 2.2UF
C2 2.2UF
IR1
HEADER_1X5
IRRX
IRTX
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JP2	PC BEEP SELECTION
1-2 ON	TRADITIONAL
3-4 ON	CONTROLLED by AC97 CODEC

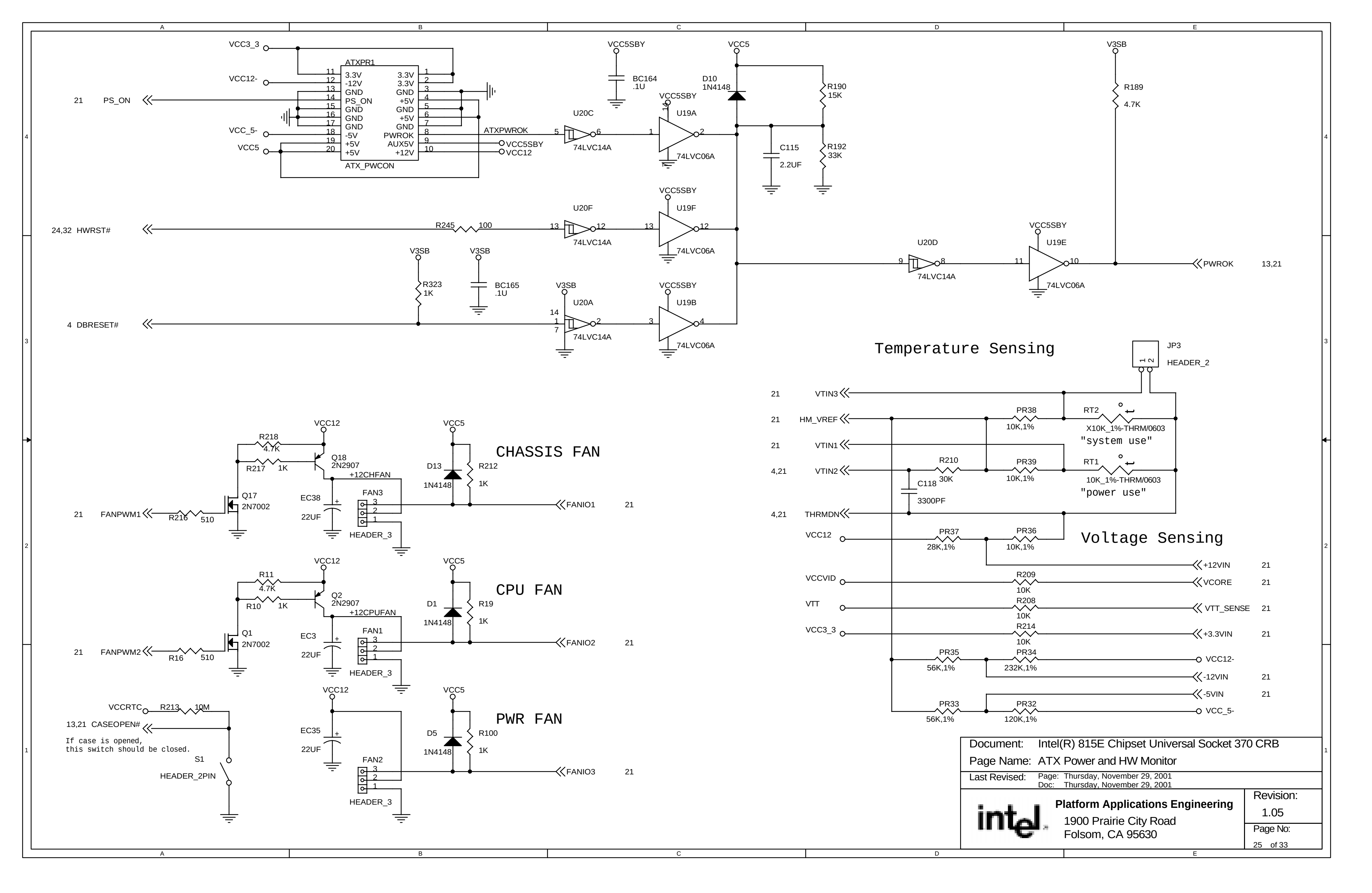
Document: Intel(R) 815E Chipset Universal Socket 370 CRB

Page Name: Front Panel Headers and CNR

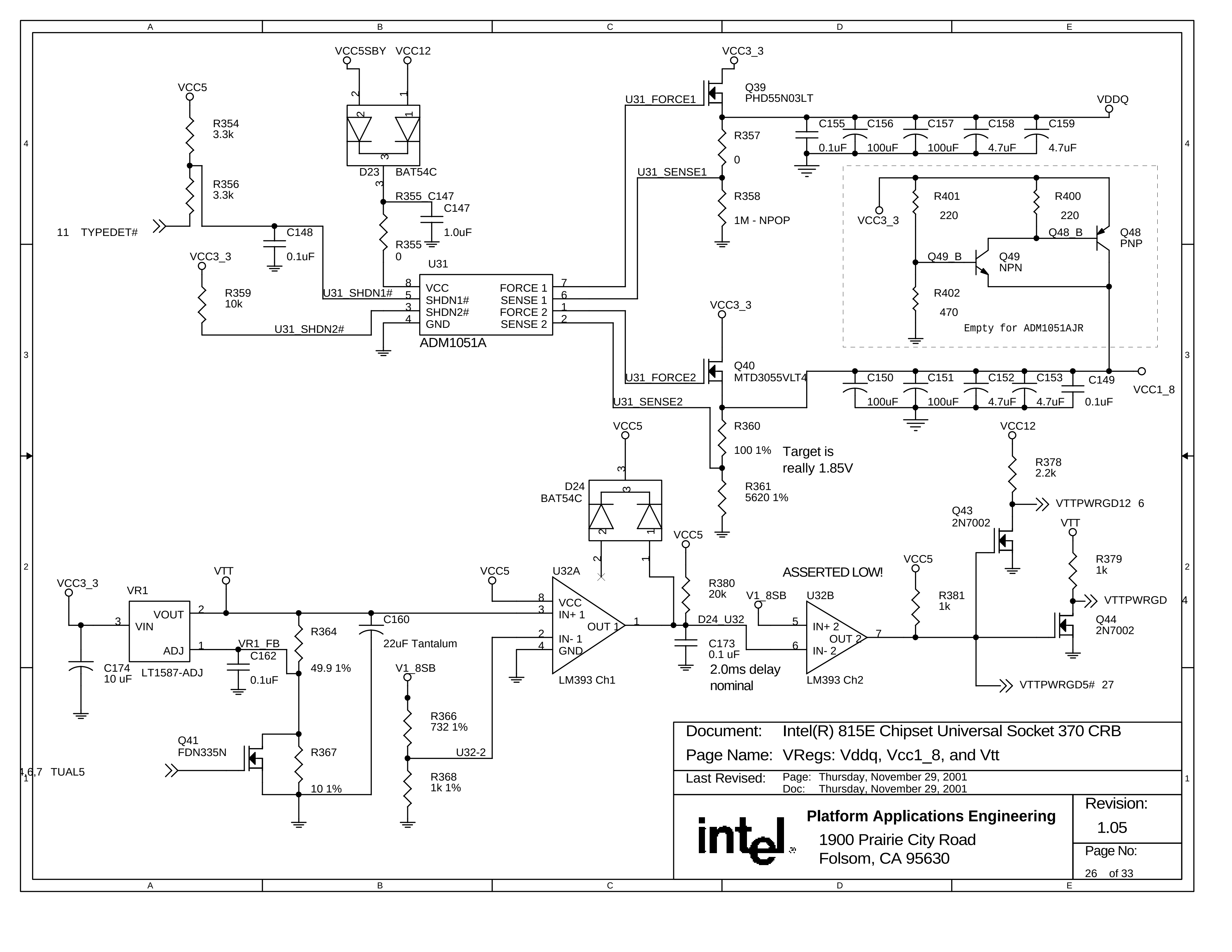
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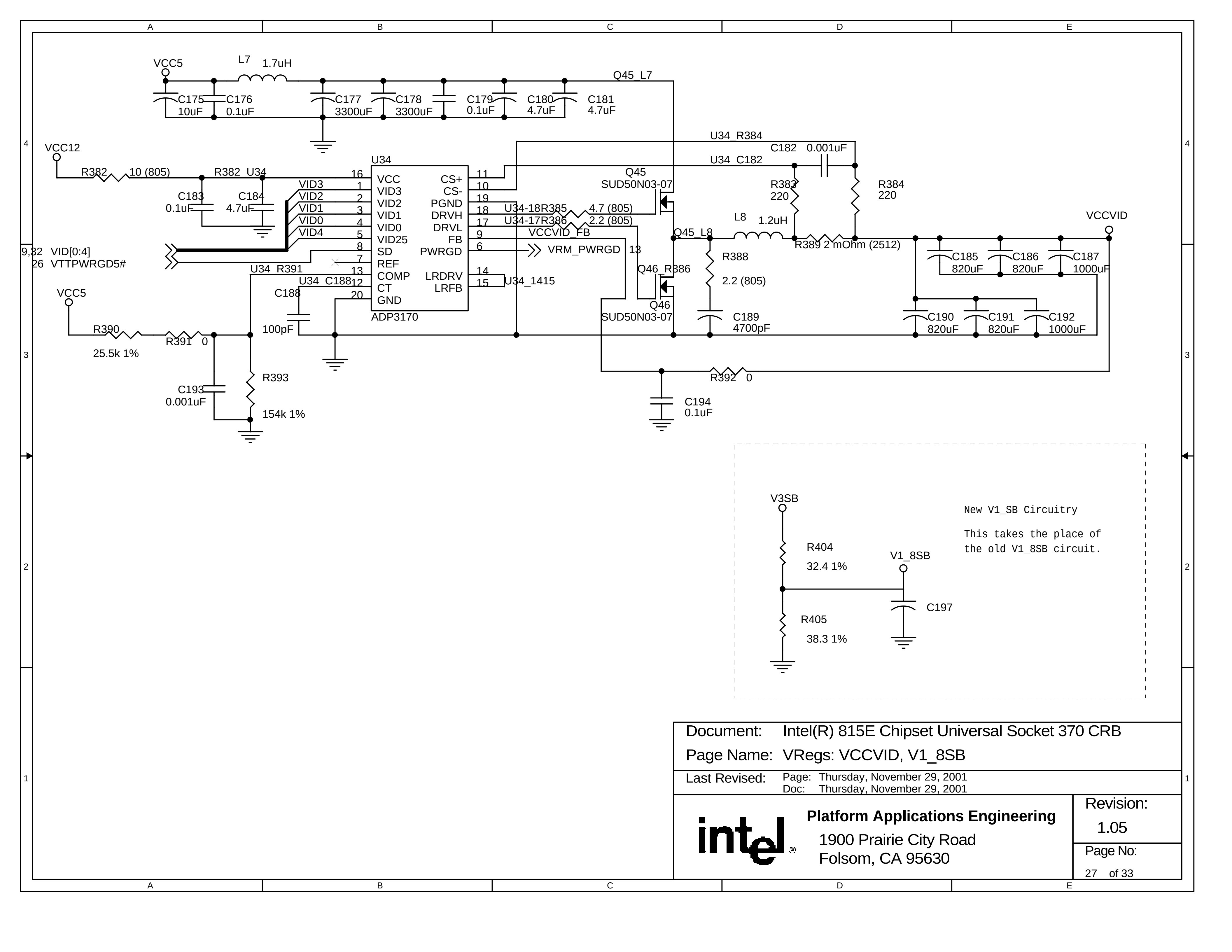
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ATXPR1
ATX_PWCON
PS_ON
HWRST#
DBRESET#
ATXPWROK
PWROK
Temperature Sensing
Voltage Sensing
CHASSIS FAN
CPU FAN
PWR FAN
VTIN3
HM_VREF
VTIN1
VTIN2
THRMDN
X10K_1%-THRM/0603
"system use"
10K_1%-THRM/0603
"power use"
+12VIN
VCORE
VTT_SENSE
+3.3VIN
-12VIN
-5VIN
FANIO1
FANIO2
FANIO3
FANPWM1
FANPWM2
CASEOPEN#
If case is opened,
this switch should be closed.
HEADER_2PIN
HEADER_3
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VCC5SBY
VCC12
VCC3_3
Q39
PHD55N03LT
U31_FORCE1
VDDQ
VCC5
R354
3.3k
C155
C156
C157
C158
C159
R357
0.1uF
100uF
100uF
4.7uF
4.7uF
D23
BAT54C
0
R356
3.3k
U31_SENSE1
R355_C147
R358
R401
R400
C147
1M - NPOP
VCC3_3
220
220
11 TYPEDET#
C148
1.0uF
Q48_B
Q48
PNP
R355
0.1uF
0
Q49_B
Q49
NPN
VCC3_3
U31
R359
10k
VCC
FORCE 1
U31_SHDN1#
SHDN1#
SENSE 1
R402
SHDN2#
FORCE 2
U31_SHDN2#
GND
SENSE 2
470
Empty for ADM1051AJR
ADM1051A
VCC3_3
Q40
MTD3055VLT4
U31_FORCE2
C150
C151
C152
C153
C149
VCC1_8
U31_SENSE2
100uF
100uF
4.7uF
4.7uF
0.1uF
VCC5
R360
VCC12
100 1%
Target is
really 1.85V
R378
2.2k
D24
BAT54C
R361
5620 1%
VTTPWRGD12 6
Q43
2N7002
VCC5
VTT
VCC5
R379
1k
ASSERTED LOW!
VTT
VCC5
U32A
R380
20k
VCC3_3
VR1
V1_8SB
U32B
R381
1k
VTTPWRGD 4
VOUT
IN+ 1
IN+ 2
Q44
2N7002
VIN
C160
OUT 1
D24_U32
OUT 2
R364
IN- 1
VR1_FB
C162
ADJ
GND
22uF Tantalum
C173
0.1 uF
IN- 2
C174
10 uF
LT1587-ADJ
49.9 1%
0.1uF
V1_8SB
LM393 Ch1
2.0ms delay
nominal
LM393 Ch2
VTTPWRGD5# 27
R366
732 1%
Q41
FDN335N
R367
U32-2
4,6,7 TUAL5
R368
1k 1%
10 1%
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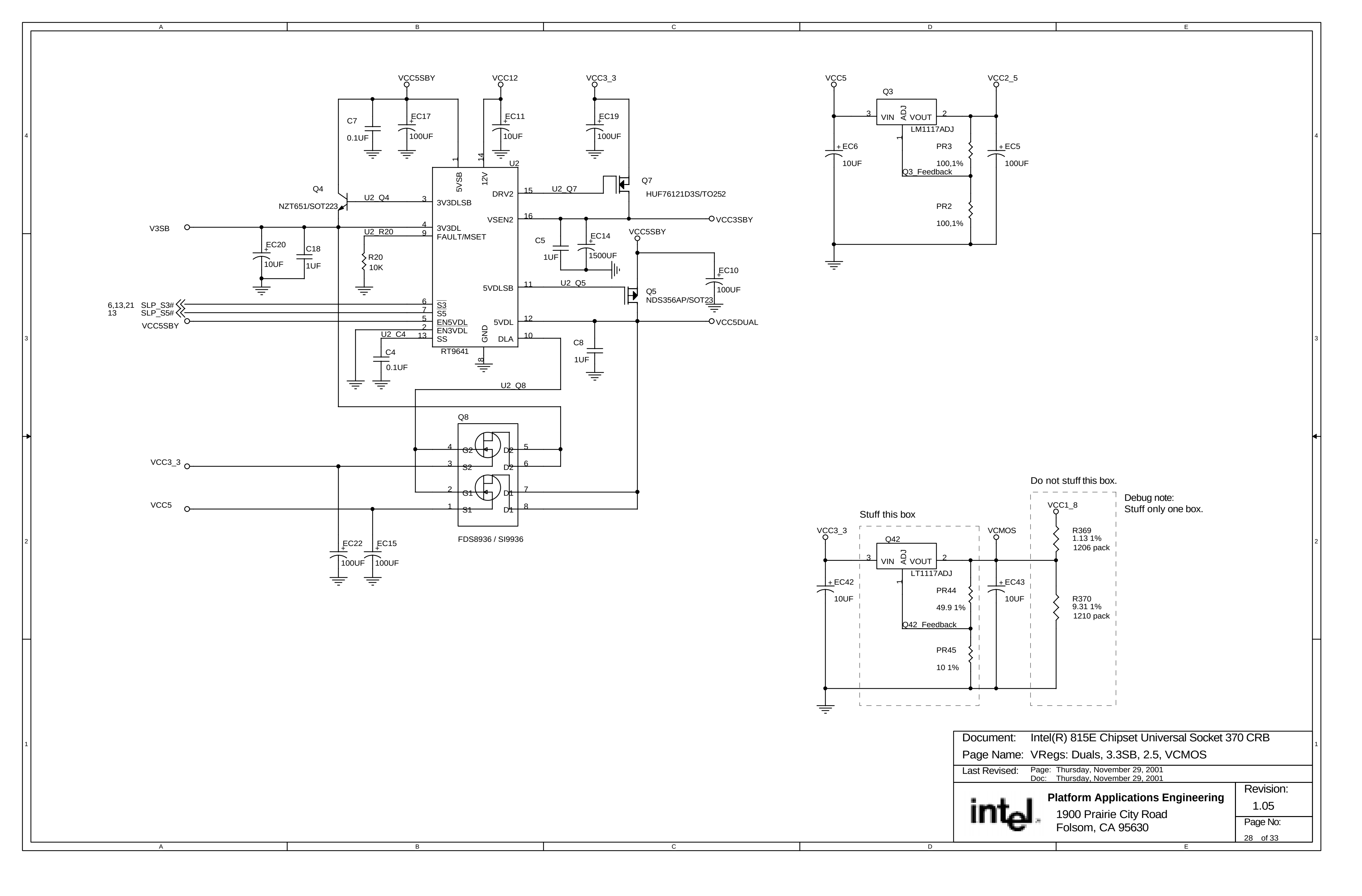
Document:	Intel(R) 815E Chipset Universal Socket 370 CRB
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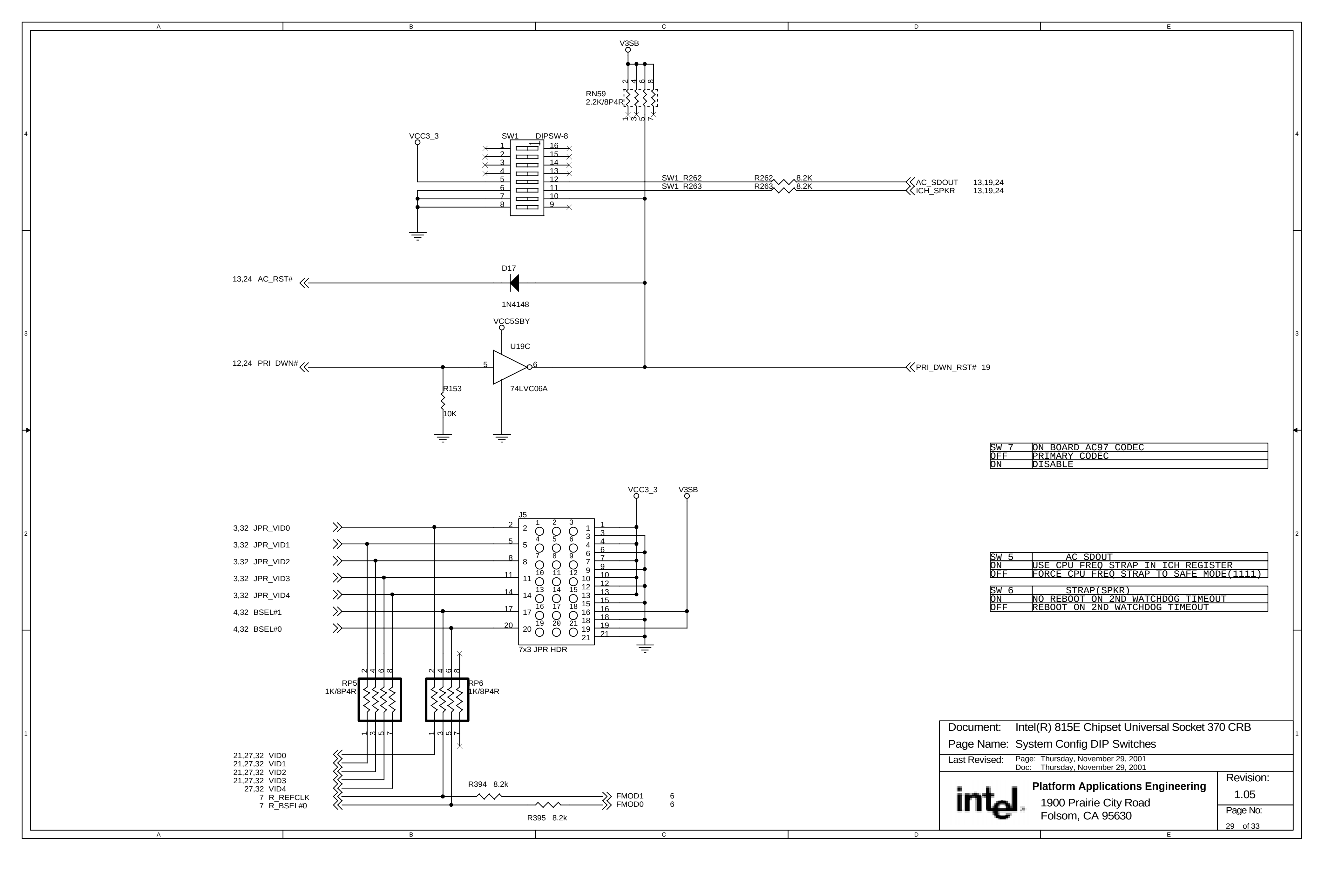


Document:	Intel(R) 815E Chipset Universal Socket 370 CRB
Page Name:	VRegs: Duals, 3.3SB, 2.5, VCMOS
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SW 7	ON BOARD AC97 CODEC
OFF	PRIMARY CODEC
ON	DISABLE

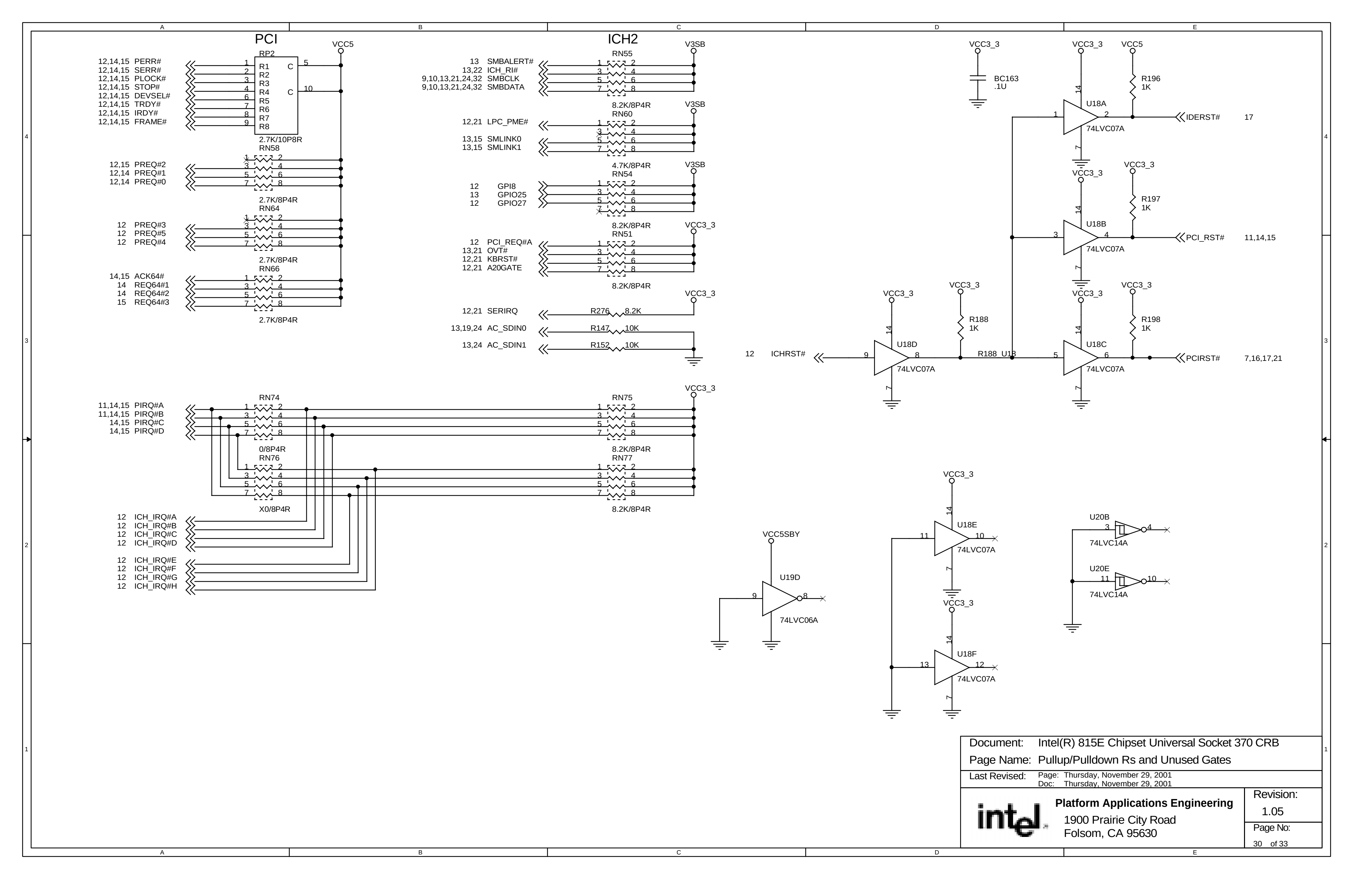
SW 5	AC_SDOUT
ON	USE CPU FREQ STRAP IN ICH REGISTER
OFF	FORCE CPU FREQ STRAP TO SAFE MODE(1111)

SW 6	STRAP(SPKR)
ON	NO REBOOT ON 2ND WATCHDOG TIMEOUT
OFF	REBOOT ON 2ND WATCHDOG TIMEOUT

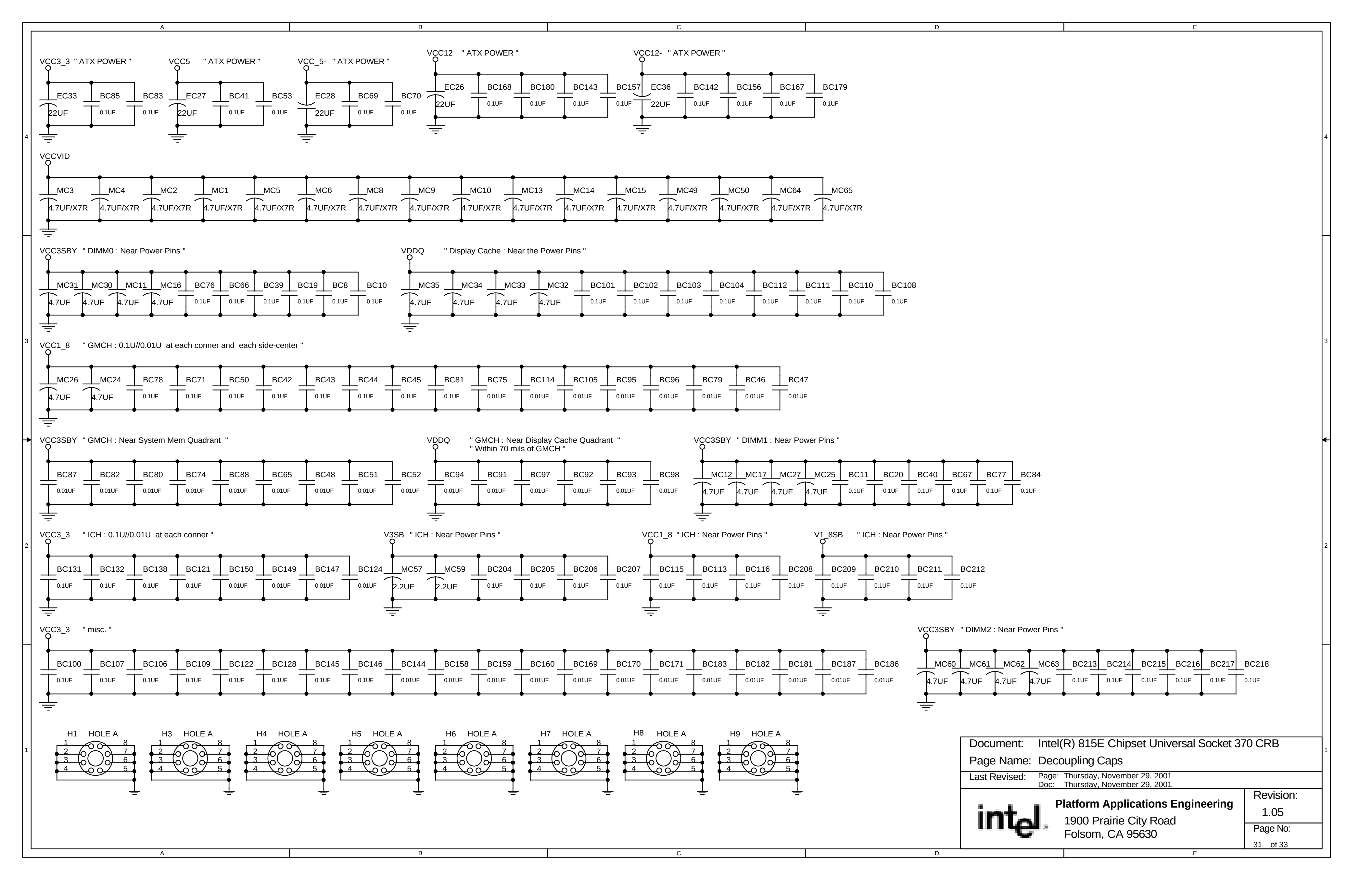
Document: Intel(R) 815E Chipset Universal Socket 370 CRB
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PCI
ICH2
RP2
VCC5
12,14,15 PERR#
12,14,15 SERR#
12,14,15 PLOCK#
12,14,15 STOP#
12,14,15 DEVSEL#
12,14,15 TRDY#
12,14,15 IRDY#
12,14,15 FRAME#
2.7K/10P8R
RN58
12,15 PREQ#2
12,14 PREQ#1
12,14 PREQ#0
2.7K/8P4R
RN64
12 PREQ#3
12 PREQ#5
12 PREQ#4
2.7K/8P4R
RN66
14,15 ACK64#
14 REQ64#1
14 REQ64#2
15 REQ64#3
2.7K/8P4R
V3SB
RN55
13 SMBALERT#
13,22 ICH_RI#
9,10,13,21,24,32 SMBCLK
9,10,13,21,24,32 SMBDATA
8.2K/8P4R
RN60
12,21 LPC_PME#
13,15 SMLINK0
13,15 SMLINK1
4.7K/8P4R
RN54
12 GPI8
13 GPIO25
12 GPIO27
8.2K/8P4R
VCC3_3
RN51
12 PCI_REQ#A
13,21 OVT#
12,21 KBRST#
12,21 A20GATE
8.2K/8P4R
12,21 SERIRQ
R276 8.2K
13,19,24 AC_SDIN0
R147 10K
13,24 AC_SDIN1
R152 10K
RN74
RN75
11,14,15 PIRQ#A
11,14,15 PIRQ#B
14,15 PIRQ#C
14,15 PIRQ#D
0/8P4R
RN76
8.2K/8P4R
RN77
X0/8P4R
8.2K/8P4R
12 ICH_IRQ#A
12 ICH_IRQ#B
12 ICH_IRQ#C
12 ICH_IRQ#D
12 ICH_IRQ#E
12 ICH_IRQ#F
12 ICH_IRQ#G
12 ICH_IRQ#H
BC163
.1U
U18A
74LVC07A
R196
1K
IDERST# 17
U18B
74LVC07A
R197
1K
PCI_RST# 11,14,15
12 ICHRST#
U18D
74LVC07A
R188
1K
R188 U18
U18C
74LVC07A
R198
1K
PCIRST# 7,16,17,21
VCC5SBY
U19D
74LVC06A
U18E
74LVC07A
U18F
74LVC07A
U20B
74LVC14A
U20E
74LVC14A
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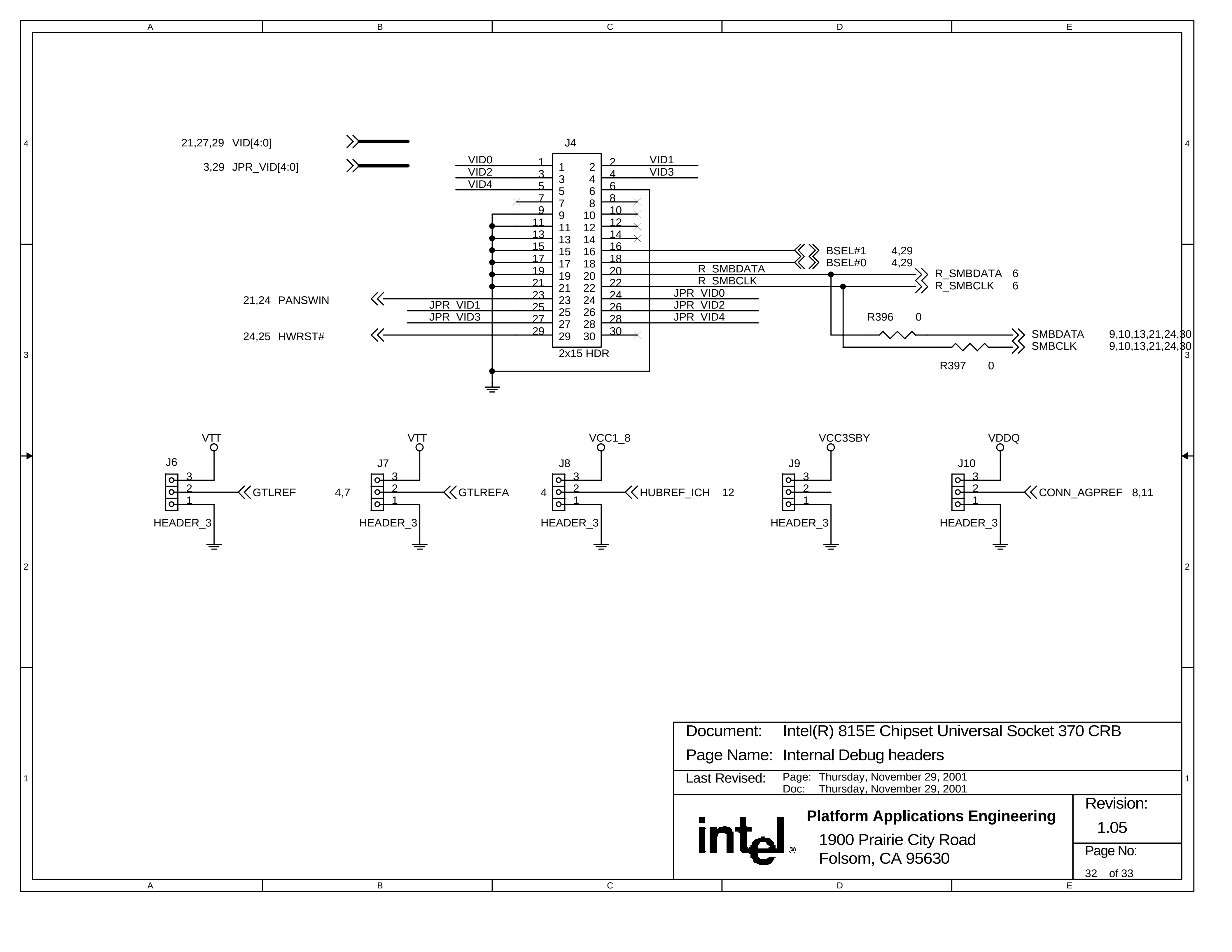
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Page Name:	Decoupling Caps
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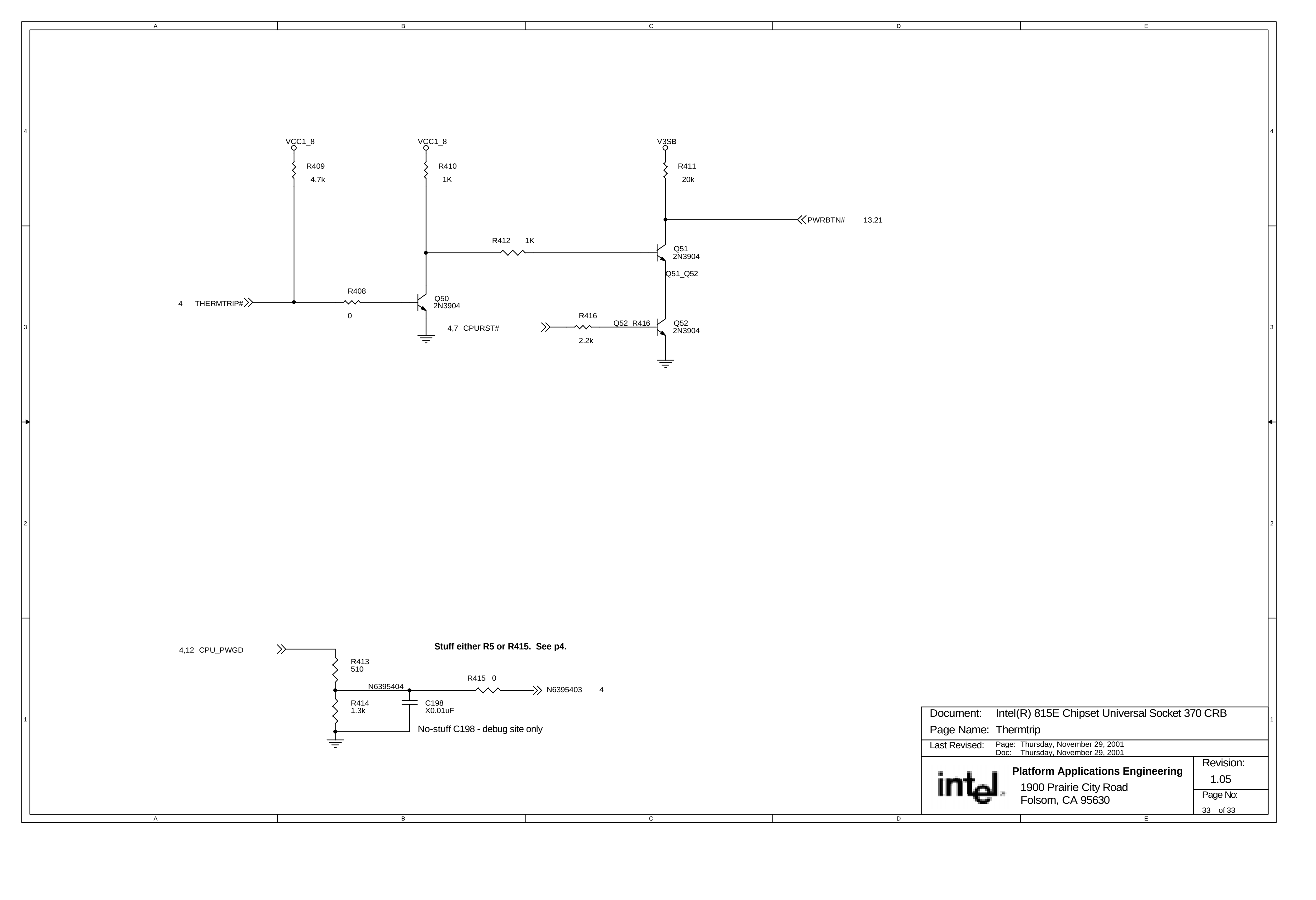
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A B C D E
4 3 2 1
21,27,29 VID[4:0]
3,29 JPR_VID[4:0]
J4
VID0
VID2
VID4
VID1
VID3
2x15 HDR
21,24 PANSWIN
24,25 HWRST#
JPR_VID1
JPR_VID3
JPR_VID0
JPR_VID2
JPR_VID4
BSEL#1 4,29
BSEL#0 4,29
R_SMBDATA
R_SMBCLK
R_SMBDATA 6
R_SMBCLK 6
R396 0
R397 0
SMBDATA 9,10,13,21,24,30
SMBCLK 9,10,13,21,24,30
VTT
J6
GTLREF
HEADER_3
VTT
J7
4,7
GTLREFA
HEADER_3
VCC1_8
J8
4
HUBREF_ICH 12
HEADER_3
VCC3SBY
J9
HEADER_3
VDDQ
J10
CONN_AGPREF 8,11
HEADER_3
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